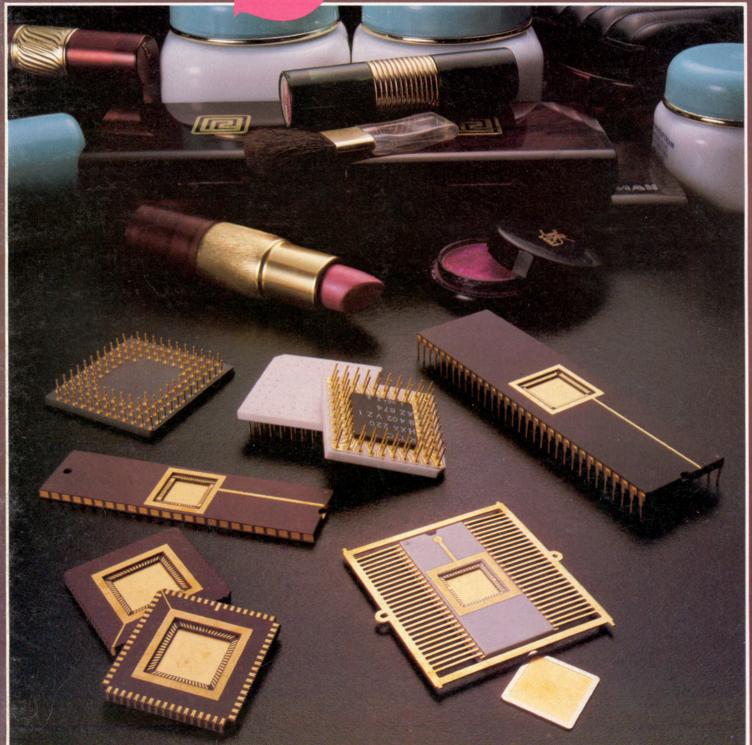


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VLSI DESIGN was founded to explore, expand, and define the interrelations between very-large-scale integrated circuits (VLSI) and computer architecture, design strategies, costs, and aids, as well as the electronics industry as a whole. VLSI DESIGN is unique in that it is written by and for the participants in this dynamic field. VLSI DESIGN intends to be the communication focus of a new VLSI design community, encourage its development, and help define its directions.



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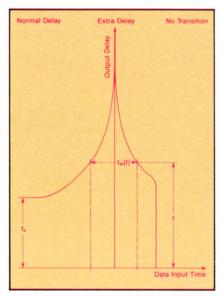
#### Cover

Although VLSI packages are often quite attractive, their selection is not merely a matter of cosmetics. VLSI designers must go beyond simple pin-count and package "footprint" considerations, and look into power dissipation, parasitics arising from dieto-package wiring, and the ease of mounting VLSI devices on printed-circuit boards. Cover photo by Jay Carlson, San Francisco, CA. LSI/VLSI packages provided by Signetics Corporation, Sunnyvale, CA.

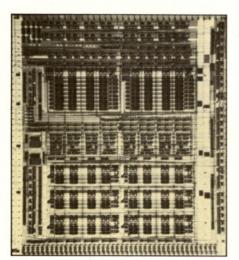


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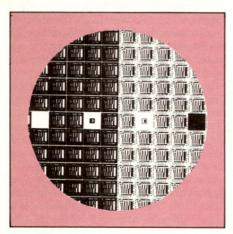
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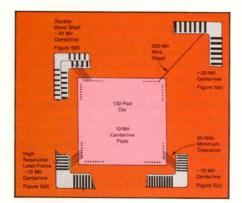
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### 16 A High-Performance Configurable Microprocessor

David Bondurant, Michael Kopman, Michael Kalm, and Philip Bytheway, Honeywell, Inc., Solid State Electronics Division

The authors explain how and why they designed a single macro-cell-based chip that can be "configured" by metal-mask changes into several different high-performance microprocessors. Although this may sound like a standard gate-array approach, it's really quite different.

### VHSIC: The Focus Shifts from Microns to Systems

Jerry Werner, Editor-in-Chief

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#### 28 Five Pitfalls to Avoid When Obtaining Optical Photomasks

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#### 36 Interfacing with E-Beam Mask Suppliers

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The authors explain the intricacies of doing business with electron-beam-mask suppliers. The article includes a table listing all U.S. merchant-market e-beam mask makers and their capabilities.

#### Practical Considerations in VLSI Packaging

S. Ralph Parris and John A. Nelson,

**Burroughs Corporation** 

Dual-inline packages (DIPs) clearly are unsuitable for LSI/VLSI devices that require more than 64 pins; but no standard package has yet emerged for high-pin-count ICs. The authors describe the design/performance ramifications of the most popular VLSI packaging alternatives.