

VLSI

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DESIGN

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Who will become the next "Yokozuna" in VLSI design?

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VLSI DESIGN was founded to
explore, expand, and define the
interrelations between very-large-
scale integrated circuits (VLSI)
and computer architecture,
design strategies, costs, and
aids, as well as the electronics
industry as a whole. VLSI
DESIGN is unique in that it is
written by and for the
participants in this dynamic
field. VLSI DESIGN intends to
be the communication focus of a
new VLSI design community,
encourage its development, and
help define its directions.

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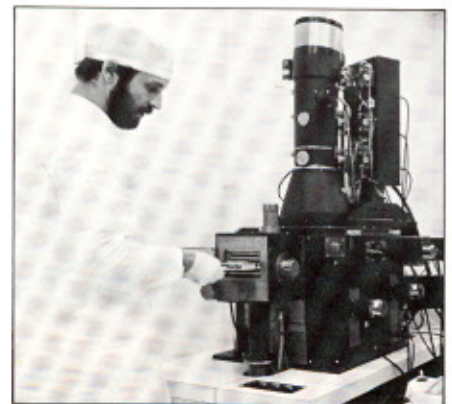
Cover

A "grand champion" Sumo wrestler is called a "Yokozuna." Japanese IC makers (who inevitably are also large computer or telecommunications makers) hope to achieve Yokozuna status by borrowing some ideas, and perfecting others. Cover illustration by Kazuhiko Sano, San Francisco, California.



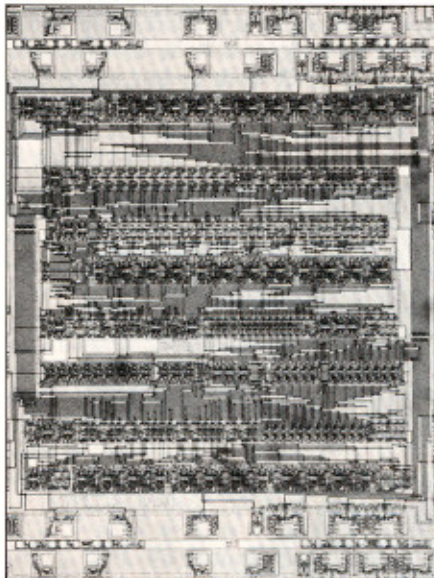
Departments

- 4 Calendar
- 8 Letters
- 10 From the Editor
- 12 People
- 30 Designer's Corner
- 50 Technology Insight
- 56 University Scene
- 66 Literature Review
- 68 Advertisers' Index



Page 56

Articles



Page 14

14 A VLSI DESIGN Special Report: Computer-Aided Design and Design Automation for ICs in Japan

Jerry Werner, *Editor-in-Chief*

Some believe that Japanese IC-makers are "strong in hardware—weak in software." This report, the result of a recent visit to Japan by *VLSI DESIGN'S* editor-in-chief, should help clarify the matter.

39 A Hierarchical Preview of the 1982 Design Automation Conference

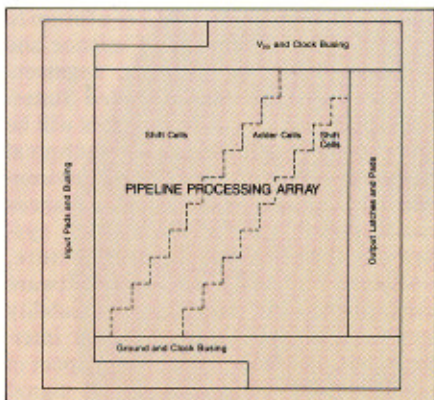
The DAC is getting so overwhelmingly large that it, like the subject of so many of its presentations (VLSI design), can benefit from a hierarchical analysis.

44 A Custom nMOS Chip for Medical Ultrasound

J. Peter Stonestom, *Unimation, Inc.*

Weston A. Anderson, *Varian Associates, Inc.*

Using a technique known as *pipelining*, the authors designed a Mead-Conway style nMOS IC for a phased-array ultrasonic imaging system. The chip operates at clock speeds greater than 20 MHz.



Page 44

60 A Constrained Design Methodology for VLSI

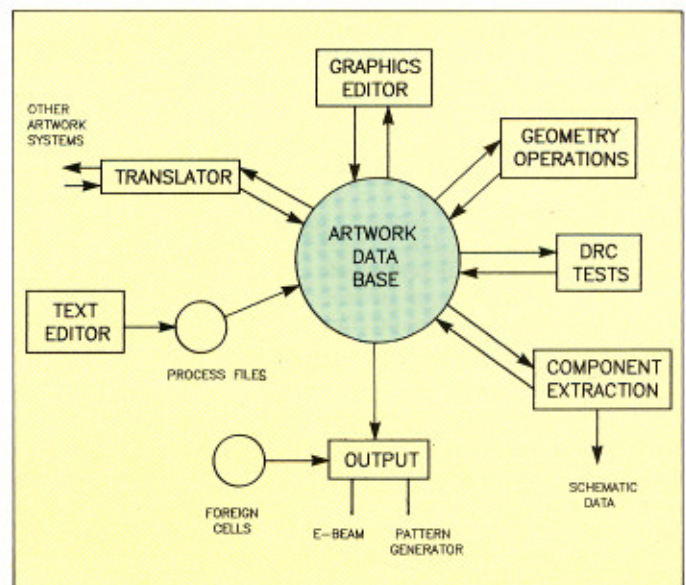
Mike Tucker, *Hewlett-Packard Company*

Lou Scheffer, *Valid Logic Systems, Inc.*

Believing that the use of overlapping cells in VLSI design reduces the effectiveness of hierarchical CAD tools, the authors propose an alternative approach that allows hierarchical verification yet exacts no penalty in chip area.

1:30	5	6	7	8
2:00	Bell Laboratories Designer's Workbench	Routing I	Special Hardware Simulation Machines	WORKSHOP Industrial Robotics
2:30	Colosseum VI	Colosseum VII	Colosseum V	Colosseum II
3:00	Coffee			
3:30	9	10	11	8
4:00	Automation in the Creation of the IBM 3081	Routing II	PLA Design Techniques	WORKSHOP (continued) Industrial Robotics
4:30	Colosseum VI	Colosseum VII	Colosseum V	Colosseum II
5:00				
5:30				

Page 39



Page 60