LAMBDA

The Magazine of VLSI Design
Second Quarter 1981

Victor Budnik

Rapid progress is now being made in computer-aided design for VLSI.

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LAMBDA was founded to explore, expand, and define the interrelations between very-large-scale integrated circuits (VLSI) and computer architecture, design strategies, costs, and aids, as well as the electronics industry as a whole. LAMBDA is unique in that it is written by and for the participants in this dynamic field. LAMBDA intends to be the communications focus of a new VLSI design community, encourage its development, and help define its directions.

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Volume II, No. 2
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Cover

The cover illustrates some of the progress we've made in VLSI design automation over the past decade. We are finally learning how to effectively describe VLSI layouts at representation levels higher than primitive rectangles and polygons. We're also making a great deal of progress in our ability to verify the correctness of these designs, whatever the method used to generate them. Several articles in this issue focus on recent progress made in design automation for VLSI. (Drawing instruments courtesy of the Oakland Museum History Department; CAD photo courtesy of Applicon Corporation; photography by Victor Budnik)

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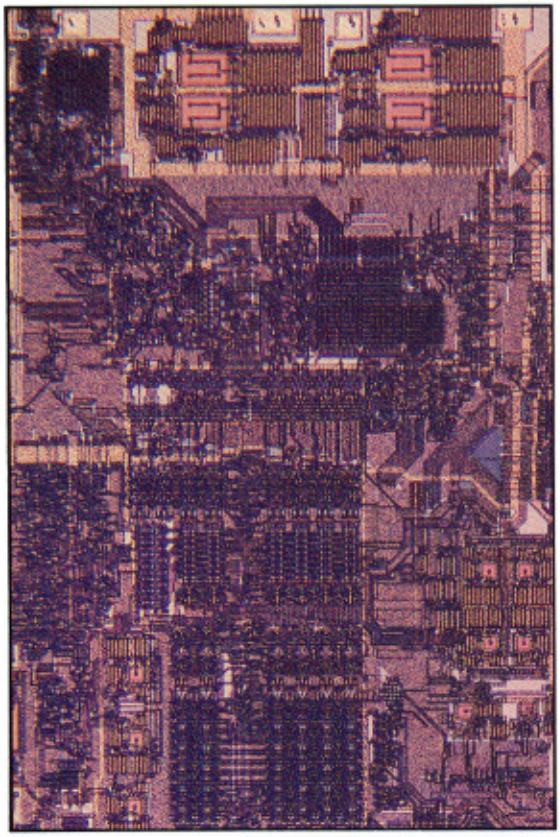

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Articles

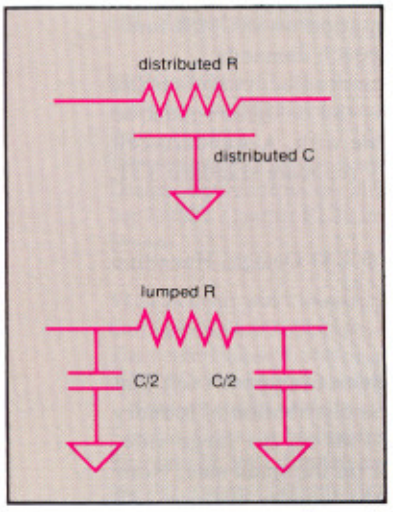
16 Stumbling Blocks to Gate-Array Acceptance

Gate-array vendors identify some major stumbling blocks to a much wider acceptance of this technology. Gate-array users are asked to comment.

20 SLIM: A Simulation and Implementation Language for VLSI Microcode

John Hennessy, *Stanford University*

The use of microcoded control structures on VLSI chips is growing rapidly. This article presents a detailed example of an excellent tool for generating and simulating this critical part of the design.



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30 What to Expect From New VLSI CAD Systems

Four prominent vendors in the field give some hints about what will soon be coming off the line.

34 A Methodology for VLSI Chip Design

William W. Lattin, John A. Bayliss, David L. Budde, Justin R. Rattner, William S. Richardson, *Intel Corporation*

The folks who brought you the iAPX 432 describe the design methodology and CAD tools they used in designing this complex chip set.

46 Benefits of Quick-Turnaround IC Processing

Merrill W. Brooksby, Patricia L. Castro, and Fred L. Hanson, *Hewlett-Packard Company*

Many perceive that a fast-turnaround processing line only benefits the designer. In this article, the authors show that fast-turnaround has inherent benefits to the processing facility itself.

52 Measuring VLSI Design Productivity

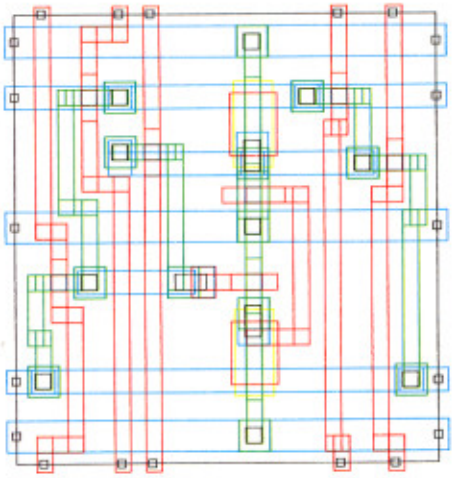
Larry Lopp, *Focused Productivity*

Mr. Lopp projects the required improvement in VLSI design productivity over the next five years in order to keep up with changes in technology.

64 Symbolic Artwork Systems

John Williams, *Consultant*

Symbolic design has attracted a lot of attention lately; this article clarifies the differences between the various approaches.



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From the Publisher

LAMBDA is well into its second year of publicaton, and the acceptance and growth of the magazine are most encouraging. Please continue to forward any news or article suggestions you may have. We are always on the lookout for good material. In recognition of our readers' strong interest in design-automation tools and methodologies, this issue contains an unusual number of articles on this and related topics.

The article from Intel, describing the design-automation system developed for use in the design of the Intel 432 micromainframe, is especially valuable because of the hard data and design experience associated with those tools. In conjunction with this article, we introduce our first "center-fold" featuring color photographs of the first three chips in the 432 family. We thought that the detailed structure of these chips was an interesting lesson in chip design, and that the photos would also make suitable wall hangings. If you have suggestions for future center-folds, please let us know.

Larry Lopp takes a look at the design-automation challenge in general, and suggests a model for predicting how fast we must improve designer productivity over the next five years to keep up with fabrication technology. You may question his assumptions or his results, but, either way, we hope you find the article thought-provoking. If you have specific comments on, or criticisms of this or any article, please write to us.

Symbolic layout systems are gaining widespread attention from both commercial vendors and university researchers. John Williams, creator of the first dynamic symbolic layout system while a graduate student at M.I.T. in 1978, surveys the field for us and offers some insight into the differences between the various systems under development.

John Hennessy of Stanford University describes the system he has developed to aid the design, layout, programming, and simulation of programmable logic arrays (PLAs). There should be enough detail in the article to help you determine what features you may want to build into your own system.

To complete this special issue on CAD, we asked each of the principal IC-CAD vendors to submit a brief summary of its view of the IC-design problem. We think you will find these perspectives different and enlightening.

Getting away from design automation, Merrill Brooksby and his colleagues at Hewlett-Packard describe the techniques and advantages of reducing the turnaround time in an IC processing line. We have often spoken of the advantages of such a line to the *designer*, but shorter turnarounds are also advantageous to those running the line.

Darryl Schofield has written an interesting article on the stumbling blocks to the wider acceptance of gate arrays. User and vendor preceptions of the problem are not necessarily the same.

For our next issue, we're planning a survey of design-automation tools for gate arrays, and a detailed look at an in-house gate-array design system that has been used with great success. We'll also have two articles on some exciting new chip designs, as well as a variety of other topics that we think you'll find well worth your attention.

Douglas G. Fairbairn

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Publisher