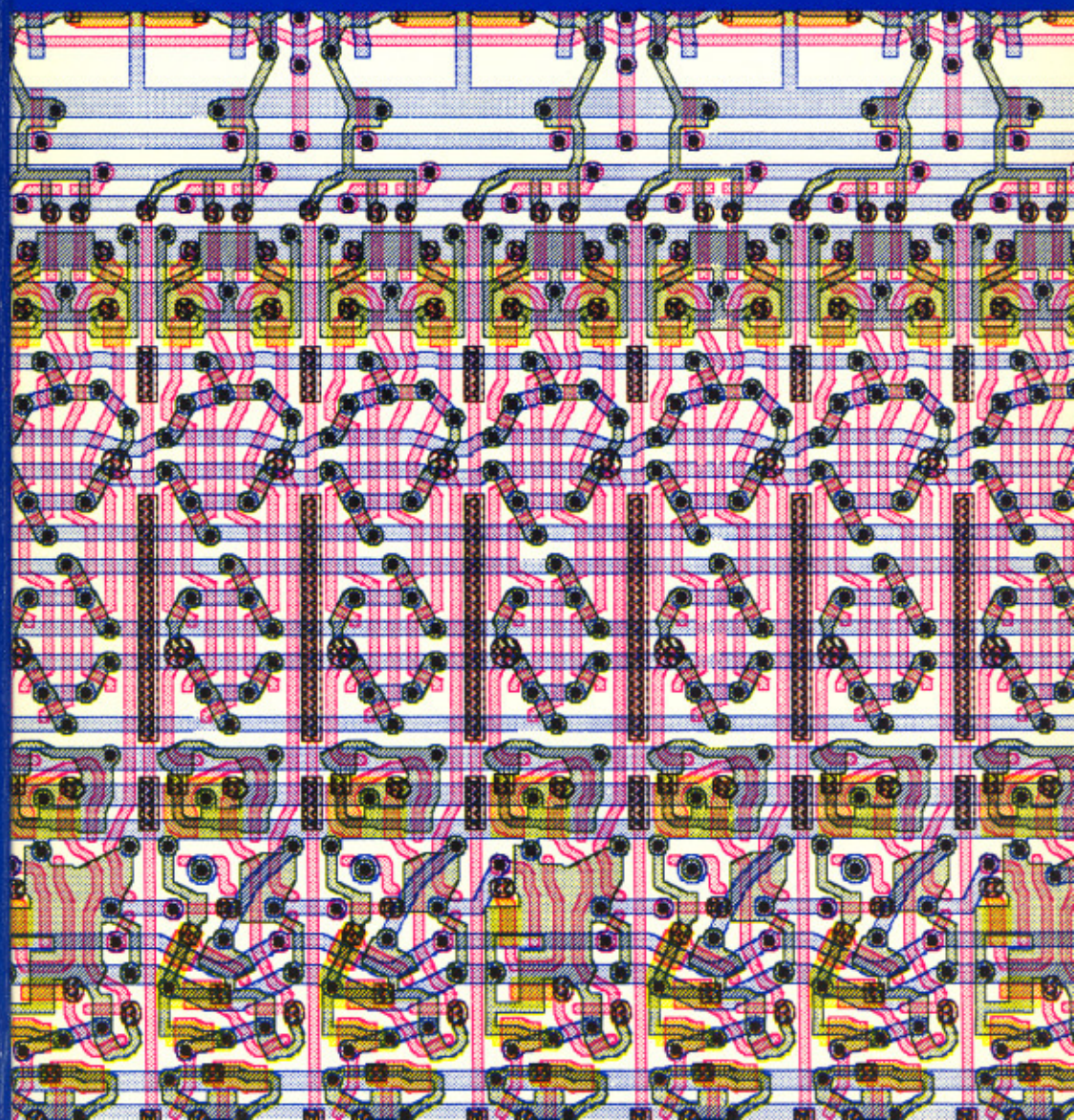


THIRD CALTECH CONFERENCE ON
**VERY LARGE SCALE
INTEGRATION**

Edited by Randal Bryant



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VERY LARGE SCALE
INTEGRATION**

Editor

RANDAL BRYANT

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Preface

The papers in this book were presented at the *Third Caltech Conference on Very Large Scale Integration*, held March 21-23, 1983 in Pasadena, California. The conference was organized by the Computer Science Department, California Institute of Technology, and was partly supported by the Caltech Silicon Structures Project.

This conference focused on the role of systematic methodologies, theoretical models, and algorithms in all phases of the design, verification, and testing of very large scale integrated circuits. The need for such disciplines has arisen as a result of the rapid progress of integrated circuit technology over the past 10 years. This progress has been driven largely by the fabrication technology, providing the capability to manufacture very complex electronic systems reliably and at low cost. At this point the capability to manufacture very large scale integrated circuits has exceeded our capability to develop new product designs quickly, reliably, and at a reasonable cost. As a result new designs are undertaken only if the production volume will be large enough to amortize high design costs, products first appear on the market well past their announced delivery date, and reference manuals must be amended to document design flaws.

Recent research in universities and in private industry has created an emerging science of very large scale integration. This science covers a wide variety of subjects, including formal models of the behavior and performance of digital systems, systematic and algorithmic approaches to computer-aided design, and new architectures and interconnection strategies to exploit the capabilities of VLSI. By providing a forum for this research, we hope this conference and these proceedings can contribute to the field and stimulate further research and new ideas.

The book is divided into seven sections, according to the sessions at the conference.

Invited Papers

Four distinguished researchers from industry and academia were invited to present their work and the insights they have gained from designing large chips. Hörbst, Sandweg, and Wallstab describe the problems faced by their research group at Siemens in designing two VLSI chips and the solutions

they adopted. Anceau presents a silicon compiler to generate chip designs automatically from a specification of the algorithm to be implemented. Hennessy, et al present the design of the MIPS processor, a microprocessor with a novel approach to instruction pipelining that promises to yield higher performance than traditional designs. Dobberpuhl discusses some of the issues faced by circuit designers in designing VLSI chips.

Circuit Timing

Traditionally, circuit designers estimate the speed of a circuit manually or by extensive circuit simulation, and find ways to improve its performance using guesswork and intuition. The papers in this session describe algorithmic approaches to performance analysis and optimization that potentially reduce the effort and amount of expertise required to design high performance chips. Both Ousterhout of U.C. Berkeley and Jouppi of Stanford describe programs that estimate the speed of circuits fabricated in nMOS technology. These programs can be used to identify regions of the circuit requiring further optimization to meet the desired clock rate. The similarities and differences of their two programs provide insight into the range of possible solutions to the problem. Leiserson, Rose, and Saxe present an algorithm for improving the performance of a circuit by finding an optimal rearrangement of the combinational logic and the registers.

Routing and Interconnection

The authors in this section describe some new algorithms and fundamental results for connecting together the different components of a VLSI system. Both Chan and Pinter address the subject of automatic wire routing, in which a computer program determines the layout of the interconnecting wires based on a specification of which terminals are to be connected. Chan presents a new algorithm for channel routing in which connections are made from one set of components to another set across a rectangular wiring channel. Pinter presents some fundamental results and algorithms for river routing, in which all wires run on the same layer (no crossovers). Greene and El Gamal, on the other hand, investigate the problem of interconnecting components in a system which is so large (wafer-scale), that some percentage of the fabricated components are defective and hence must be bypassed after fabrication. Their paper describes methodologies for designing restructurable systems and some statistical analyses of their reliability.

Formal System Models

Models of the behavior of digital systems form the basis of techniques for synthesizing and verifying VLSI systems. For example, a logic simulator has some model of the operation of a digital system as its basis. A variety of models have been proposed, differing greatly in generality, accuracy, practicality, and mathematical rigor. The papers in this section present research on the more mathematical side of system models. Shostak describes a method using temporal logic to verify the correct operation of a digital system based

on assertions about the behavior of the individual components. Chen and Mead describe a simulator that can model a system at several levels of abstraction from the transistor level description up to a functional description. Rem, van de Snepscheut, and Udding present trace theory as a formal model for describing the behavior of concurrent systems. And then van de Snepscheut describes a method for synthesizing a circuit based on a specification of its desired behavior in terms of its trace structure.

System Building Blocks

The construction of a large system is greatly facilitated by a design methodology in which components obeying a set of interface conventions are connected according to a set of composition rules to yield a subsystem with well-defined behavior. The papers in this section illustrate two such methodologies: self-timed systems in which the components communicate according to an asynchronous protocol, and systolic systems in which the components operate in tight synchrony. Hayes presents a design system for realizing self-timed, finite state controllers using a cellular design method called PPL's. Frank and Sproull describe the design of a static RAM chip using self-timed protocols. Finally, Fisher, et al describe a chip which can be used to construct highly parallel architectures based on the systolic approach, with the functionality of the architecture determined both by the interconnection structure and the programming of the individual chips.

Special-Purpose Chip Architectures

Many algorithms can be performed at a much higher speed when implemented directly in hardware rather than as software on conventional computers. Such algorithms form attractive applications for computer-aided custom VLSI design, because neither high chip density nor carefully optimized circuits are required to produce a system with higher performance than would otherwise be available. Furthermore, the design of special-purpose chips often leads to new architectures with applications beyond the original problem. In this section Truong, et al describe the design of a chip for encoding data to be sent from a deep space satellite to Earth. Such an application clearly has performance, weight, and power constraints that only a custom VLSI chip can provide. By careful selection of the encoding and multiplication algorithms, they were able to fit the entire encoder on a single chip. Schaeffer, Powell, and Jonkman describe several approaches to the design of special-purpose hardware for generating the set of legal moves from a particular board position in chess. This problem consumes a large portion of the computation time in chess-playing programs and lends itself well to some unusual architectures. Ja'Ja' and Owens describe ways to reduce the amount of processor hardware in systems consisting of many interconnected processors operating in parallel. It is shown that for certain problems a relatively small number of processors accessing a large number of memory elements can achieve high performance.

Silicon Compilation

The term "silicon compiler" is applied to a large variety of computer programs that synthesize chip designs directly from a specification of either the functionality, the logic design, or the circuit schematic. The building blocks used by the compiler to generate the layout can range from arbitrary geometry to a library of parameterized standard cells. Furthermore, silicon compilers differ greatly in their range of applications and in the flexibility of their floorplans. Wolf, et al describe a very general program that transforms a circuit schematic into a stick diagram which can then be compacted to yield a layout. Both Pope and Broderick as well as Bergmann present silicon compilers specifically designed to produce chips for signal processing, with one using parallel arithmetic and the other using bit-serial. By focusing on a particular class of applications, these compilers can produce designs with high performance and density.

Acknowledgments

This conference and proceedings have benefited from the efforts of many people. Clearly the authors deserve most of the credit, because their efforts to carry out research and report the results form the basis of the conference. The members of the program committee served to define the direction of the conference and reviewed many papers in a short amount of time. The other reviewers also aided greatly in the paper selection process. Chuck Seitz of Caltech and both Paul Penfield and Barbara Lory of MIT shared much of their wisdom gained from organizing previous VLSI conferences. Linda Getting and Pam Hillman handled most of the administrative aspects of organizing and running the conference. Finally, the staff of the Caltech Computer Science Department including Phyllis Weiss, Vivian Davies, Dianne Hahn, and Helen Derevan spent many hours handling the large amount of paperwork required to put on such a major event.

Cover Illustration

The illustration on the cover shows part of the layout for the tree machine processor designed at Caltech by Chuck Seitz, Don Speck, Steve Rabin, and Peter Hunter. This design was written in the layout language EARL in which the design is specified as a hierarchical composition of cells. The lowest level (leaf) cells consist of a set of geometric objects that are required to satisfy a set of programmer-defined spacing constraints. These cells are composed by stretching the geometry subject to the constraints so that the ports of adjacent cells align. Close inspection of the layout will show examples of wires which have been specified as paths which must miss other objects by minimum radii, and cells which have been composed by stretching. This layout also illustrates the use of "Boston" geometry in which lines at arbitrary angles and circular arcs are permitted. Recent extensions to EARL enable the designer to produce "Manhattan" geometry in which only lines parallel to the X and Y coordinate axes are permitted, providing better compatibility with existing pattern generators and design rule checkers.

R.E. Bryant, January, 1983

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ABOUT THE BOOK

The papers in this book were presented at the *Third Caltech Conference on Very Large Scale Integration*, held March 21-23, 1983 in Pasadena, California. The conference was organized by the Computer Science Department, California Institute of Technology, and was partly supported by the Caltech Silicon Structures Project. This conference focused on the role of systematic methodologies, theoretical models, and algorithms in all phases of the design, verification, and testing of very large scale integrated circuits. The papers span a wide range of topics including formal models of the behavior and performance of digital systems, systematic and algorithmic approaches to computer-aided design, and new architectures and interconnection strategies to exploit the capabilities of VLSI. This book provides a view into the emerging science of very large scale integration, a science which will permit electronic systems to be designed with higher performance and reliability and at a lower cost than is possible today.

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