Proceedings of Caltech Conference on

VERY LARGE SCALE INTEGRATION

PROCEEDINGS

of the Caltech Conference on

VERY LARGE SCALE INTEGRATION

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FOREWORD

Integrated circuit fabrication technology has advanced in the past 15 years from the capability of producing a few to producing tens of thousands of switching devices interconnected on a single silicon chip. It is well understood what has made the advance from the integrated logic gate to the integrated processor possible. Improvements in the fabrication technology have reduced the density of defects, which makes larger chips feasible. At the same time these improvements have increased the density of circuitry by making transistors and wires much smaller. Reduced size also results in faster and/or lower power operation.

This progress has been so steady that the microelectronics industry has come to expect and to count on it. Very Large Scale Integration (VLSI) is a projection, a promise, a prophesy, that the evolution from Small Scale Integration (SSI) to Medium Scale Integration (MSI) to Large Scale Integration (LSI) will be followed by something even grander. Indeed, there is every reason to expect the trend to increased function on single chips to continue. The physical theory of semiconductor devices indicates that transistors as small as 1/20th of today's typical 5 micron dimensions would still function. Hence an additional increase in density of about 400 times is possible before any fundamental limits are reached. There is a practical rather than absolute limit to the size of chips, based on the best balance between yield and complexity. Optimum chip size is generally projected to increase.

This scaling of the fabrication technology promises such enormous returns in computing, defense, instrumentation, communication, and consumer electronics applications that aggressive research programs have been initiated in universities and in industry both here and abroad. One major segment of this

research is directed toward the development of fabrication and lithographic techniques to produce circuits whose parts are even smaller than a wavelength of visible light. While it is the fabrication technology which appears most closely related to achieving the goal of VLSI, even the present art may be more severely limited by the ability to design than the ability to fabricate circuits. The other major segment of VLSI research is concerned with methods for managing the design of systems composed of very large numbers of switching elements, and information system applications and architectures which are well adapted to VLSI.

This conference was organized to provide a broad view of the research efforts underway both in industry and in universities. Caltech has been a pioneer in education and research in integrated circuit and system design, and we at Caltech are pleased to have been able to provide a forum for the diverse and interesting work reported at the conference and in these *Proceedings*. The attendance of nearly 500 people, more than three times as many as had been expected in our early planning based on the largest previous attendance at a conference sponsored by the Caltech Industrial Associates, was gratifying in the size of the response, but particularly in its distribution. The mix of people from universities, government, and industry was as apparent at the conference as it is in the authorship of the papers in these *Proceedings*.

The opening session of the conference was devoted to presentations by keynote and invited speakers, and was arranged to provide an overall view of the economic, engineering, scientific, and mathematical issues and aspects of the field. Although we invited these leaders in the field to speak without any obligation to prepare written material for these *Proceedings*, most speakers have provided papers or abstracts derived from their notes or from tape transcriptions.

The next two days of the conference were devoted to five

technical sessions: fabrication, innovative LSI designs, computer-aided design, self-timed logic, and architecture. The papers presented were selected from nearly twice as many submitted. The organization of these sessions and the paper selections were the responsibilities of the session chairpersons, Lynn A. Conway, Robert F. Sproull, William R. Heller, Charles E. Molnar, and J Craig Mudge. The chairpersons have also provided an introduction to each of the sessions for these *Proceedings*.

The overall organization of the conference was undertaken by the undersigned pair, members of the Caltech computer science faculty, but most of the work was done by Tom Walters, director of the Industrial Associates Office, by the Caltech public events people, and by our secretaries, Donna Glaviano and Janice Patterson. These *Proceedings* were edited by Chuck Seitz, with a lot of help from Donna Glaviano and Chris Hankins.

Charles L. Seitz

John P. Gray