Conference on Advanced Research in VLSI, Massachusetts Institute of Technology

This conference, the fourth in a series that since 1979 has alternated between MIT and Caltech, included 10 invited talks and 21 contributed papers.

At 8:45 a.m. on the opening day of the conference (January 25), MIT Professor Paul Penfield, Jr., welcomed the attendees and set the stage for the following three days of nearly non-stop activity. MIT president Paul E. Gray then brought the audience up to date on the status of the $16 million (in 1981 dollars) "VLSI Research Laboratory," to be housed in a renovated building on the MIT campus. The laboratory, as announced at a similar MIT conference in January 1980, was originally intended to be a pilot line for class-project chips. However, the purpose of the laboratory has since changed, Gray said. When complete, the lab will be used to fabricate only those devices that cannot be handled by then-existing silicon foundries.

The laboratory now has committed funds of just under $10 million–somewhat short of the original $16 million estimate. Nonetheless, the final go-ahead has been given to the architect, Gray said. (The lab is now targeted for completion in 1984.)

One of the highlights for conference attendees was the opening-day banquet, held on the Discovery, *a floating pavilion located next to the New England Aquarium. Enjoyable sea-lion and dolphin performances preceded the excellent dinner. For an added touch of humor, the dolphins were named (at least for this one performance) "Carver" and "Lynn."*

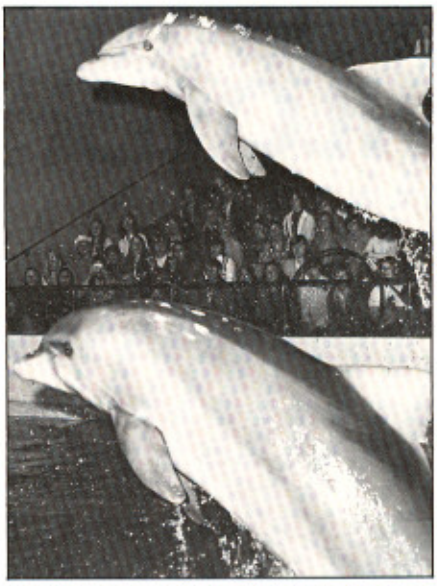
Below is a synopsis of the presentations:

"The Interaction of VLSI Theory and Practice: A Case Study," Jon Louis Bentley, Carnegie-Mellon University, Pittsburgh, PA

"Overview of Processing and Materials Technology for Si LSI/VLSI in Japan," Yasutaka Ban, Fujitsu Limited, Kawasaki, Japan

"Wavefront Array Processor: Architecture, Language, and Applications," S.Y. Kung, R.J. Gal-Ezer, K.S. Arun, Department of Electrical Engineering. Univ. of Southern California, Los Angeles, CA

This paper describes the development of a Wavefront Array Processor (WAP),



Carver (bottom) and Lynn entertain MIT conference attendees. *(Photo courtesy of the New England Aquarium.)*

which provides a powerful tool for the high speed execution of a large class of matrix operations and related algorithms.

"A 0.1 μm CMOS/SOS Inverter Simulated via a New MOS Scaling Approach," Donald C. Mayer and Richard C. Henderson, Hughes Laboratories, Malibu, CA

This paper describes a general approach to MOS scaling that determines an optimized performance path through a multidimensional parameter space. This approach eliminates the constraints, such as constant field or constant voltage, imposed by conventional MOS scaling techniques. A test implementation predicts successful CMOS/SOS inverter operation down to 0.1 μm gate length (operating range is 0.5 to 1.0V).

"Generating Custom High-Performance VLSI Designs from Succinct Algorithmic Descriptions," Jeffrey Mark Siskind, Jay Roger Southard, Kenneth Walter Crouch, MIT Lincoln Lab., Lexington, MA

The design process of an IC can be viewed as the successive refinement of higher-level descriptions into lower-level ones. This paper discusses a compiler which converts programs in a language known as MacPitts directly to mask level specifications for chips using microprogram sequenced data-path operations.

"Effect of VLSI on Programming Languages," Alan J. Perlis, Yale University, New Haven, CT

"High Performance VLSI Computer Packaging," C.H. Ho, IBM T.J. Watson Research Center, Yorktown Heights, NY

"The Partitioning of Concerns in Digital System Design," Mark Stefik, Daniel G. Bobrow, Alan Bell, Harold Brown, Lynn Conway, and Christopher Tong, VLSI System Design Area, Xerox PARC, Palo Alto, CA and Heuristic Programming Project, Stanford Univ., Stanford, CA

This paper proposes the use of explicit abstraction levels to organize decision making in digital design. These levels partition the concerns that a designer must consider at any time. They provide terms and composition rules for the composition of structural description within a level. This allows multiple opportunities for mapping behavior into structure.

"Datapath Design for RISC," Robert W. Sherburne Jr., Manolis G.H. Katevenis, David A. Patterson, and Carlo H. Séquin, EECS, Computer Science Division, University of California, Berkeley, CA

The data path of RISC I is described, with special emphasis on the register file and the shifter. The layouts of the two particularly compact versions of these modules are presented, and the trade-offs in their design as well as simulation results are discussed.

"Timing Verification of VLSI Logic Circuits," David W. McSweeney, NCR, Wichita, KS

This paper describes how a set of computer programs are being utilized to check nMOS logic-circuit designs for timing errors. The programs find the paths which could cause timing errors, and calculate the delays along these paths.

"Architecture Oriented Objects," Iann M. Barron, INMOS Ltd., Bristol, United Kingdom

"High Speed Silicon Integrated Circuits Using X-ray Lithography," M.P. Lepselter, Bell Laboratories, Murray Hill, NJ

"The SCHEME-81 Architecture—System and Chip," John Batali, Edmund Goodhue, Chris Hanson, Howie Shrobe, Richard M. Stallman, and Gerald Jay Sussman, The Artificial Intelligence Laboratory, Massachusetts Institute of Technology, Cambridge, MA

SCHEME-81 is a large-scale microprocessor designed at MIT to directly interpret SCHEME, a high-level language. SCHEME-81 is designed to support a novel organization where computers are specialized by including hard-

ware to accelerate their performance on particular problems and where communities of computers are interconnected to solve large problems.

"TEM Studies of VLSI Circuits," R.B. Markus and T.T. Sheng, Bell Laboratories, Murray Hill, NJ

An important element in VLSI processing is the ability to reveal morphological features on chips which cannot be predicted. This identification becomes more critical and more difficult as dimensions shrink to 1 μm and below. Transmission electron microscopy (TEM) studies of cross-sections of VLSI circuits can now be used to supply this information, which is hard or impossible to obtain by other methods.

"Exploiting Structure in Integrated Circuit Design Analysis," Martin E. Newell, Xerox PARC, Palo Alto, CA, Daniel T. Fitzpatrick, Xerox PARC, and Computer Science Division, University of California, Berkeley, CA

This paper presents a general approach to exploiting hierarchy and repetition in the analysis of integrated circuit designs, and includes details of a circuit-extraction algorithm that uses this approach.

"VLSI—From Here to Reality," Donald S. Beilman, General Electric Co., King of Prussia, PA

"VLSI Memory: A Designer's Viewpoint," Richard C. Foss, MOSAID, Inc., Ottawa, Canada

The author contends that the design and development of VLSI memories is not well understood, even within broad-product-range semiconductor companies. This paper reviews some key factors in VLSI memory design.

"Hierarchical Design Validation Based on Rectangles," Stephen C. Johnson, Bell Laboratories, Murray Hill, NJ

This paper discusses a system that uses design hierarchy and signal connectivity information, applied to the basic rectangles that make up the geometric design, to perform high-speed logical validation of circuits.

"Analog to Digital Conversion Using Sigma-Delta Modulation and Digital Signal Processing," Jeffrey R. Fox, GTE Laboratories Inc., Waltham, MA; G.J. Garrison, Microtel Pacific Research Ltd., Burnaby, B.C., Canada

The authors contend that the technique of digital signal processing (DSP) will gain greater acceptance to perform functions formerly implemented in an analog fashion. This paper describes a voice-band 13-bit sigma-delta DSP analog-to-digital converter, suitable for integration in a 5-micron or less nMOS depletion load, or CMOS technology.

"Systolic Networks for Orthogonal Equivalence Transformations and Their Applications," Don E. Heller, Ilse C.F. Ipsen, Computer Science Department, Penn. State University, University Park, PA

Systolic arrays, as conceived by Kung and Leiserson, are a useful tool for special purpose VLSI system design. The authors show how to design systolic arrays for the QR factorization of a banded matrix, hence solving of linear least squares problems, and how to perform iteration for eigenvalues and singular values.

"A Computational Array for the QR-method," Lennart Johnsson, Computer Science Dept., California Institute of Technology, Pasadena, CA

The QR-method solves a linear system of equations. The matrix R is upper triangular and Q is a unitary matrix. This paper describes a concurrent algorithm and corresponding array for computing the triangular matrix R by Householder transformations.

"Ensemble Architectures for VLSI—A Survey and Taxonomy," Charles L. Seitz, Computer Science Dept., California Institute of Technology, Pasadena, CA

Over the past several years, much of the work at Caltech has been concerned with systems that are ensembles of identical, concurrently operating, and regularly interconnected elements. From these investigations, a pattern and taxonomy of this one class of VLSI architectures is beginning to emerge.

"The Role of VLSI-CAD in the Fifth Generation Computer Project," Tohru Moto-oka, University of Toyko, Tokyo, Japan

"Developing Pixel-Planes, a Smart Memory-Based Raster Graphic System," Henry Fuchs, John Poulton, Department of Computer Science, University of North Carolina at Chapel Hill, NC; Alan Paeth, Alan Bell, VLSI System Design Area, Xerox PARC, Palo Alto, CA

The authors describe recent developments of pixel-planes, a smart memory-based raster graphic system designed to support graphical interaction with 3D color rendered surfaces at a level that today is only possible with simple "wire-frame" line drawings.

"Automated Design of Switched-Capacitor Filters," Phillip E. Allen, Otto N. Fanini and Liem T. Nguyen, Department of Electrical Engineering, Texas A&M University, College Station, TX

A method under development is described which will permit the automatic design of switch-capacitor filters using pre-processed silicon wafers. The approach makes use of a repeated building block connected in a manner determined by the design algorithm.

"Systolic Stacks, Queues, and Counters," Leo J. Guibas, Xerox PARC, Palo Alto, CA; Frank M. Liang, Computer Science Dept., Stanford Univ., Stanford, CA

The authors describe new systolic algorithms for the implementation of stacks, priority queues, and counters in large-scale integrated circuits. These designs allow new operations to be performed with constant delay, independent of size of the data structure.

"PLATES: A Metric-Free VLSI Layout Language," Sarma Sastry and Steve Klein, USC, Information Science Institute, Marina del Rey, CA

The authors present a layout description language that frees a designer from the need to verify design rule constraints and determine absolute object coordinates. Designs can be specified in a technology-independent manner, and the design rules are enforced elsewhere.

"The Data Path Generator," Howard E. Shrobe, MIT, Artificial Intelligence Laboratory, Cambridge, MA

The author describes an experimental design system which constructs a novel data path for machines which directly implement interpreters or similar procedures on a microprocessor chip. The system enables the layout of a large data path such as that of the SCHEME-81 microprocessor, to be accomplished in approximately 30 minutes of elapsed time.

"Processor Displacement: An Area-Time Tradeoff Method for VLSI Design," David M. DeRuyck, Lawrence Snyder, John D. Unruh, Computer Science Dept., Purdue University, West Lafayette, IN

The authors contend that direct VLSI implementation of pipelined (systolic) processor arrays can lead to an "over-parallelized" chip having unused or under-utilized area. They describe "processor displacement"—a methodology that provides a spectrum of designs with differing time/area trade-offs.

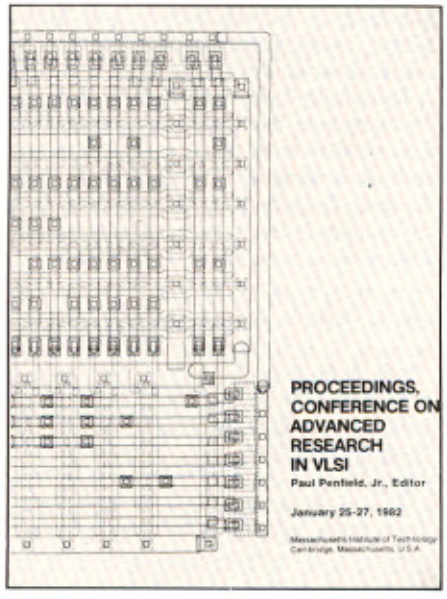
"Physical Simulation of Bipolar Device Structures," J.L. D'Arcy, G.T. Pearman, E.J. Prendergast, and P. Lloyd, Bell Laboratories, Allen, PA

This paper examines the development and use of steady-state and AC small-signal physical simulators for the two-dimensional modeling of basic bipolar device structures. The results presented suggest that physical simulation has potential as the primary basis for the devel-

opment of compact models used for circuit level simulations, with measurements assuming an essential but supporting role.

"Sakura: a VLSI Modeling Language," Norihisa Suzuki, Xerox PARC, Palo Alto, CA; and Rod Burstall, Xerox PARC and Edinburgh University, Scotland

The authors describe a VLSI modeling language based on a powerful system-description language. The main features of this language are: (1) abstraction, which allows one to split a system arbitrarily, (2) functional specification, which is completely separated from the implementation, and (3) structural specification, which describes the connection.



The 1982 MIT Proceedings, Conference on Advanced Research in VLSI *is available from:*

Artech House, Inc.
610 Washington Street
Dedham, MA 02026
(617) 326-8220
$34 (includes UPS shipping)

Purdue Update

Professor Gerry W. Neudeck, from the E.E. Dept. of Purdue, sent us these descriptions of a new VLSI design course (to be offerred in the spring of 1982) and a graphics package called "MASK."

EE559: "MOS VLSI Design"

This course touches on most of the aspects of VLSI MOS integrated circuit design, namely:

1. Device fabrication and modeling;
2. Useful circuit building blocks;
3. System considerations, and
4. Algorithms to accomplish common tasks.

Most circuits are treated in detail; particular attention is given to circuits whose regular and/or expandable structures make them prime candidates for integration. Most circuits are digital, and almost all are considered in the context of Si-gate MOS enhancement/depletion-mode technology.

The goal of this course is to introduce the basics of VLSI design within the context of a modern methodology, and to expose students to many circuit and subsystem building blocks.

Course text book: C.A. Mead and L.A. Conway, *Introduction to VLSI Systems*, Reading, MA, Addison-Wesley Publishing Co., 1980.

Purdue "MASK" Graphics Package

The layout of VLSI circuits requires a computer-graphics package to reduce the time-consuming process of drawing precision polygons in highly repetitive arrays. Ultimately, these polygons are produced in opaque patterns on a photo plate by a pattern generator. In producing VLSI custom integrated circuits and in device research, it is necessary to obtain photo plates quickly, and to modify the basic patterns without long delays. To reduce the turn-around time for design modification, we have developed a system in which the computer-graphics terminals are tied directly to the pattern generator via a minicomputer.

The complete graphics-to-pattern-generator system hardware consists of a digitizing board, three graphics terminals, an inexpensive flat-bed plotter, an electrostatic plotter, a pattern generator, and a PDP 11/70 or VAX minicomputer. The software is written in the "C" programming language, runs under the UNIX operating system, and is available to the public upon request. The MASK computer-graphics program includes most of the standard commands available in commercial graphics packages. However, several convenient features have been incorporated, such as the ability to write on 128 different levels, and to specify which level or combination of levels is visible on the graphics terminal or should be plotted.

Complete device layouts and logic functions may be stored in a public library or in a user's private library. Essentially any number of libraries is possible. A simple command calls a device or logic function into MASK from the library, with all drawing levels preserved. The "cell" from any library maybe positioned with the thumbwheel cursor, and set in place with one key-stroke. After repositioning with the cursor, additional cells may be repeated any number of times. When calling a cell from a library, the operator has the option of scaling, rotating and reflecting about the Y-axis. Thus, devices and logic blocks can be reproduced quickly and easily.

The MASK commands can be divided into several groups. "Drawing" commands are used to establish polygons and text (lettering). The "edge" command produces straight lines between cursor locations. A "path" command draws two parallel lines with a user-specified separation, and is particularly useful for drawing metallization paths. The "text" command provides lettering of user-specified size, and can be rotated into any quadrant.

"Edit" commands are used to change what has been drawn previously and/or to reproduce repetitive patterns such as cells. "Change element" commands identify the picture element, change its level, move it, and digitize its location. Precision drawings with large separations between picture elements cannot be placed visually. Therefore, number registers provide an option for specifying cursor locations not visible on the screen, thereby allowing precision placement of picture elements and cells.

Areas already drawn on the screen can be "picked" and placed ("put") repetitively with optional scaling and rotation.

"Drafting commands" help the operator view or gauge spacings on the screen. For example, "grid" places a drawing grid of operator specified size and origin. "Lock grid" forces all entries onto the grid, making precision location possible. "Lock axis" forces the elements to consist of only vertical and horizontal lines.

The "file manipulation commands" include a "help file" that lists the syntax of all commands. "Lib" lists the contents of the public library files or the user's library files.

Interested commerical firms may obtain MASK by sending a tape and a letter stating that they will not sell or give away the software without written permission (from the E.E. Department of Purdue), to: Gerry W. Neudeck, Ph.D., Purdue University, Electrical Engineering Building, West Lafayette, Indiana 47907.

We invite other universities, who have developed VLSI design software that potentially is useful to the industrial community, to let us know. Space permitting, we will include this information in future University Scene columns.