University Scene

Lynn Conway

There's a lot of exciting news of university VLSI design activities to report in this issue of LAMBDA - - - design environments have improved rapidly in many schools - - - courses, computing environments, and design-aid environments at 12 major universities are tabulated - - - the MPC580 network adventure was a great success - - - the Xerox-PARC VLSI implementation system technology has been successfully transferred to USC/ISI - - - plus news of courses, conferences, and other university events.

VLSI Design in the Universities

The VLSI design environments within a community of twelve U.S. universities matured very rapidly during the past school year. A detailed tabulation of the present environment at each school is given later in the column.

Project-oriented courses were offered during '79-'80 by Jonathan Allen at *M.I.T.*, John Newkirk and Rob Mathews at *Stanford Univ.*, Carver Mead and Chuck Seitz at *Caltech*, Carlo Sequin at *U. C. Berkeley*, John Murray at *Univ. of Colorado*, Colorado Springs, Jacob Abraham at *Univ. of Illinois*, Bob Sproull at *Carnegie-Mellon Univ.*, Vance Tyree at *UCLA*, John Nelson at *USC*, Frederic Rosenberger at *Washington Univ.* (St. Louis), a group of faculty at *Univ. of Rochester*, and Ted Kehl at *Univ. of Washington*, Seattle. These twelve schools then participated in the MPC79/MPC580 ARPANET adventures (see below), using the Xerox-PARC VLSI implementation system to convey their student and research projects into silicon.

One reason for rapid design-environment development was a high degree of collaboration among the schools. Often, as useful new design aids were created, they were easily and quickly shared, because many of the schools have similar computing environments. New knowledge was diffused rapidly by use of the ARPANET computer-communication network.

Another reason for rapid progress was keen competition among the schools and among individual participants. The schools share a common VLSI design culture; during '79-'80 all used the same implementation system, and batches of projects from the schools were often implemented simultaneously. Therefore, project creation, innovations in system architecture, and innovations in design aids at each of the schools have been quite visible to the others. These factors stimulated competition, which led to additional ambitious, innovative projects.

There is strong pressure in each school to have the latest, most complete set of design aids, because successful design completion (and thus participation in competition) depends on these aids. This pressure tends to counter any "not invented here" opposition to importing ideas or accepting new infrastructural standards. The forces for collaboration and for competition are thus coupled in a positive way, and there is "gain in the system". The prognosis for further rapid progress is good indeed!

Videotape Course Created

In parallel with running their course at *Stanford*, John Newkirk and Rob Mathews presented the course to a group of engineers at Hewlett-Packard. During the project phase of the course, guest lectures were presented by a number of leading VLSI researchers and architects. The entire event was organized by Doug Fairbairn, Manager of VLSI Engineering at VLSI Technology, Inc. (VTI), and Merrill Brooksby, Manager of Corporate Design Aids at HP. It was conducted in the HP television studios in Palo Alto, enabling professional-quality videotaping of all lectures. This excellent course is now commercially available from VTI.

Computing and Design-Aid Environments for Some 1980-81 VLSI Design Courses

Those familiar with software systems immediately know what you're talking about if you mention compiler, interpreter, assembler, loader, executive, etc. In the early days, a new implementation of one of these functions might receive a new "buzzword name" that obscured the nature of the function. However, a common view of these generic functions gradually emerged above the details of particular implementations. The set of functions needed to form basic but complete software environments for various purposes is now common knowledge.

A similar phenomenon is beginning in the area of VLSI design aids. Many aids of proven value, such as the circuit simulator SPICE, are well known by their buzzword names. However, the VLSI design community is increasingly aware of what *set of functions* is needed to form a basic (but complete) VLSI design environment. It is also aware of what new functions might be sought through research, in order to improve the state of the art.

The university project-labs provide an interesting environment for observing progress in design methodology. Because of competitive pressures, the project-labs often reflect the latest thinking on what constitutes a basic but complete design environment. This environment is receptive to new architectural concepts, design methods, and design aids that emerge from research work. Thus the group of project-labs provides a large social "experimental laboratory" for the reality-testing of new design methods.

We believe many **LAMBDA** readers will be interested in following the evolution of the university design environments. To this end, we've tabulated information about the twelve U.S. universities that offered project-oriented VLSI design courses last year. Included is a list of the types of design aids which support course-projects at each university during the present school year. It will be interesting to examine these environments again in the future, and perhaps then be able to sense the rate and direction of progress.

We hope these efforts at taxonomy and tabulation will stimulate discussion, and help accelerate community convergence on common terminology and common understanding. Some readers might use this table to identify environments similar to theirs, leading to early opportunities for sharing ideas and software. (In a later issue of **LAMBDA** we will tabulate specific design aids that have passed beyond the experimental phase and become available in released, supported form.) Others might be able to identify interesting targets of opportunity: areas of design-aid work where successful developments could make a big difference to many others in the community. The entries in the table are the following:

COURSE INFORMATION is given, including instructors' names, course numbers, semesters or quarters courses are offered (X-Y indicates a sequence; X, Y indicates repeat offering), and the number of students likely to attend (which often indicates the project-lab capacity).

COMPUTING ENVIRONMENTS which support the courses are sketched by listing the CPU and operating system used, and the programming language(s) usually chosen to

UNIVERSITY:	MIT	Caltech	Stanford	CMU
COURSE INFORMATION				
Instructor(s)	J. Allen, L. Glasser	C. Mead, C. Sietz	J. Newkirk, R. Mathews	R. Sproull
Course #	6.371	CS181, CS182	EE271	15-846
Sem. or Qtr.	F, Sp	F-W-Sp	F, Sp	Sp
#stud./Class	35	40	60	30
COMPUTING ENVIRONMENT				
CPU	DEC-20	DEC-20, VAX	DEC-VAX	DEC-VAX
Op. Sys.	TOPS-20	TOPS-20, UNIX	UNIX	UNIX
Prog. Lang.	LISP, APL, CLU	Simula, C	C	C
DESIGN AID ENVIRONMENT				
Synthesis aids	PLAG, MI	MG, MI	PLAG	PLAG
Description aids	SLL	SLL	SLL	SLL,IGL
Analysis aids	CX,SS, DRC,CS	CX,SS,CS	CX,DRC,SS	CX,SS,DRC
Viewing aids	CPP, BRP	CPP,CRP, CD	BRP	CPP,BRP, CD,BD
Testing aids	MTE	MTE	MTE	- - -
PROJECT EXPERIENCE (# projects, # designers)				
MPC79	15, 27	24, 28	19, 35	5, 5
MPC580	11, 13	21, 22	32, 59	12, 17

SUMMARY OF DESIGN-AID CODES:
BD: B/W Display; *BRP:* B/W Raster Plotter; *CD:* Color Display; *CPP:* Color Pen Plotter; *CRP:* Color Raster Plotter; *CS:* Circuit Simulator; *CX:* Circuit eXtractor; *DRC:* layout Design Rule Checker; *IGL:*

implement design aids. The environments at several schools are in transition; for these, the present CPU and operating system are listed first, followed by the new ones.

DESIGN-AID ENVIRONMENTS are sketched by listing the aids which support course projects. Aids are listed by generic type rather than by their "buzzword names". A simple, arbitrary taxonomy is used, with five categories of design aids, and various generic aids within each category:

(i) *Synthesis Aids:* Codes are given for aids that carry out procedural transformations of designs from higher-level descriptions into sticks or layout-level descriptions, or that assist the designer in intelligent ways during exploration of design alternatives. Examples are: PLA generators (PLAG); Sticks-to-layout Generators/Compressors (SGC); Module Generators (MG); Module Interconnectors (MI). ("Bristle-Blocks", for example, contains both an MG and an MI.) Soon to come into use are finite-state machine generators that perform state-assignment, and PLA generators that perform minimization (so we'll need to refine the encoding of these types). Over the longer term, we'll see exciting new synthesis-aid types, as current research begins to pay off.

(ii) *Description Aids:* Codes are given for the method used to encode and edit designs: Symbolic Layout Language (SLL); Symbolic Sticks Language (SSL); Interactive Graphic Layout (IGL); Interactive Graphic Sticks (IGS). Other types will be added as new synthesis aids enable higher-level representa-

U.C.B.	U. of Col. (C.S.)	U. of Illinois	U. of Wash.	U. of Rochester	UCLA	Wash. U. (St. L.)	U.S.C.
R. Newton C. Sequin	J. Murray	J. Abraham E. Davidson	T. Kehl	E. Kinnen G. Kedem	V. Tyree	F. Rosenberger	J. Nelson
CS248	EE594	EE325	CS590D	492	M258A, B, C	EE463	EE599
F	F	F, Sp	F, W, Sp	F	F-W-Sp	Sp	F
50	20	20	15	25	20	25	30
DEC-VAX,	DEC-20	HP1000	DEC-20, VAX	ALTO, VAX	DEC-VAX	DEC-20	DEC-KL10
UNIX	TOPS-20	RTE IV	TOPS-20, VMS	ALTO, UNIX	UNIX	TOPS-20	TOPS-10
C	Simula, Pascal	Pascal	FORTRAN	C, Pascal	C, Pascal	Simula, FORTRAN	Pascal
PLAG, SGC	MG, MI	- - -	PLAG, MI	- - -	- - -	PLAG	- - -
SLL, IGS	SLL	IGL	SLL	IGL	SLL	SLL	SLL
CX,SS,CS	CS	CS	DRC	CX,SS,DRC	CS	CS	CS
BRP,BD	CPP	CPP,BD	CPP	CPP,BRP, CD,BD	CPP	CPP,CD	CPP
- - -	- - -	MTE	- - -	MTE	MTE	- - -	- - -
4, 4	1, 1	5, 8	1, 3	5, 9	- - -	- - -	- - -
8, 12	12, 21	8, 13	15, 15	3, 3	9, 9	9, 11	10, 15

Interactive Graphic Layout; IGS: Interactive Graphic Sticks; MG: Module Generator; MI: Module Interconnector; MTE: Minimal Test Environment; PLAG: PLA generator; SGC: Sticks-to-layout Generator/Compressor; SLL: Symbolic Layout Language; SS: Switch Simulators; SSL: Symbolic Sticks Language.

tions to be interpreted or compiled to sticks and layouts.

(iii) *Analysis Aids:* Codes are given for the analysis aids routinely used: Circuit Extractors (CX); Switch Simulators (SS); Circuit Simulators (CS); layout Design Rule Checkers (DRC). This category will expand as register-transfer simulators, microcode simulators, etc., are brought into use in the project labs.

(iv) *Viewing Aids:* Most schools now use simple software for scaling, windowing, and plotting or displaying designs, so this category now lists only the hardware devices used to view designs: Color Raster Plotter (CRP); Color Pen Plotter (CPP); B/W Raster Plotter (BRP); Color Display (CD); B/W Display (BD).

(v) *Testing Aids:* The aids used in functional testing of chips are listed. Only a few schools now have even a "Minimal Test Environment" (MTE), consisting of a simple hardware interface and support software, so that students can do basic functional testing without extensive hardware design and breadboarding. At most schools, students are on their own, and breadboard test hardware from scratch. This is a target of opportunity for you folks out there! I hope next year to list several generic categories of testing aids being used at several schools!

PROJECT EXPERIENCE. Project completions are indicated by listing the number of projects each school submitted to MPC79 and MPC580, along with the number of partici-

pating designers. The number of schools and level of activity at each school will undoubtedly increase, now that the ISI implementation system is operational, and continuing support for university access is being provided by DARPA (and perhaps will be provided soon by NSF).

We invite your comments, criticisms, and suggestions. Do you find the table useful? How would you like to see it extended? Are there design aids in use at your school that don't fit into the taxonomy, suggesting its modification? Can you think of some new generic types beyond those listed? Write and let us know!

Summer Courses

Several schools just offered summer courses in VLSI design for the first time. Alan Bell of Xerox-PARC presented a course to 30 students at *Stanford University,* compressing a full semester's material into eight weeks. His students produced fourteen projects, which were implemented during the trial run of ISI's new implementation system (see below).

At *M.I.T.,* Jonathan Allen offered a two-week intensive course to a group of 30 students (two weeks being considered the maximum that attendees from industry can usually schedule). The first week of lectures covered the basics of VLSI design. Morning lectures during the second week covered the structure and use of contemporary VLSI design aids, while the afternoons were devoted to a novel laboratory exercise. Students were given a partially-completed design containing errors at various levels of abstraction. They used analysis aids to locate the errors, edited the design files to correct the errors, and then completed the design. This innovative technique provided an intensive design experience within a very short time period.

MPC580: Another Great Network Adventure

During the spring of 1980, another VLSI adventure was conducted over the ARPANET: the Xerox VLSI implementation system was again used to implement designs from universities and research organizations throughout the U.S. The Defense Advanced Research Projects Agency (DARPA) collaborated in the effort and provided network communications. Micro Mask, Inc. provided fast-turnaround E-beam maskmaking. Pat Castro's Integrated Circuit Processing Lab at Hewlett-Packard provided wafer fabrication. Custom packaging was done by Systems Concepts, Inc.

Throughout the spring, the Xerox system interacted via network messages with the community of designers, broadcasting instructional messages and library files, coordinating space allocations, and then receiving service-request messages from users as their designs neared completion. (For an overview of VLSI implementation systems, see the MPC79 article by Conway, Bell, and Newell in **LAMBDA**, 2nd Quarter 1980.) Xerox-PARC team members Glenn Krasner, Maureen Stone, and Wayne Wilner were led by Ted Strollo. The team was assisted by Alan Bell, principal architect of the Xerox system.

A total of 171 designs from 220 designers were received prior to the design cutoff on May 30th (from 12 universities, and also from BBN, Xerox Research, ISI, and JPL). The implementation system was operated during the next several days to plan the placement of projects into die types and mask sets, and to generate the MEBES-format mask specifications. The giant project set filled five mask sets, and required 45 different die types! Four of the mask sets contained projects at $\lambda = 2.5$ microns; the fifth contained selected projects at $\lambda = 2.0$ microns.

Maskmaking began on 6 June. HP received the first masks, and began processing on 11 June, with HP process engineer Mike Beaver supervising the wafer fabrication effort. The first wafers came off the line on 9 July. Shipments of packaged chips to designers began on 14 July. (There was about a week of pipelining of mask, fab, and packaging, due to the huge number of projects.)

At summer's end, we already have reports on the testing of 20 projects. Many of these have proved to function correctly. By far the most ambitious project in MPC580 was the RSA Encryption Chip by Ron Rivest of M.I.T. That fascinating project is described in detail in this issue of **LAMBDA**. We look forward to further reports describing many of the other innovative projects implemented via MPC580.

The New USC-ISI VLSI Implementation System

Following the MPC79 demonstration of the feasibility and advantages of VLSI implementation systems, DARPA undertook to construct and operate a similar system. The project is being led by Danny Cohen at the Information Sciences Institute (ISI) at USC. ISI staff members Ron Ayres, George Lewicki, Leroy Richardson, and Vance Tyree worked closely with Alan Bell and with

Ted Strollo's team at Xerox during MPC580 to transfer the new implementation system knowledge and technology to ISI.

The ISI system was rapidly constructed during the summer, and successfully underwent initial trials by implementing projects from the Stanford summer course, research project designs from Caltech, and test-structure prototypes from JPL and NBS.

This new implementation system will be "on the air" this fall, providing service to universities and research organizations conducting DARPA-sponsored VLSI research. At this writing, discussions are underway among DARPA, ISI, and the National Science Foundation that may lead to NSF support for access to this service by other U.S. universities.

Reports of New Courses

Henry Fuchs, of *Univ. of North Carolina*, Chapel Hill, and Tom Gallie, of *Duke University*, Durham, are jointly offering a VLSI design course this fall at UNC. The course will be offered again next spring by Peter Marinos at *Duke Univ.*, and by Harold Martin at *North Carolina A&T State Univ.*; James Gault will present the course during '81 at *North Carolina State Univ.*, Raleigh - - - Glen Miranker of IBM Research in Yorktown Heights, N.Y., is introducing a course at *Columbia University*, as are John Carr at *University of Pennsylvania* - - - Andrea LaPaugh at *Brown University* - - - Charles Kime at *University of Wisconsin*, Madison - - - Ronald Lomax at *Univ. of Michigan* - - - Phillip Allen at *Texas A&M* - - - Thomas Brubaker at *Colorado State Univ.*, Fort Collins - - - Joseph Sharp at *California Polytechnic State Univ.* - - - Amar Mukhopadhyay at *Univ. of Central Florida* - - - Noble Powell at *Cornell* - - - Frank Prosser at *Indiana University* - - - and George Williams at *Union College*.

Reports of new courses abroad: Peter Maxwell will offer a VLSI design course at *University of New South Wales*, Sydney, Australia, as will Jean Vuillemin at *University of Paris*, Orsay, France - - - D.N. Choudhury at *Indian Institute of Technology*, Delhi, India - - - M.I. Elmasery, *Univ. of Waterloo*, Ontario - - - and J.T. Wallmark at *Chalmers University*, Gothenberg, Sweden. A group of universities in the U.K. begin microelectronics design courses this year, and a plan is underway to establish a national service for implementing design projects. We'll report on these U.K. activities in detail in an upcoming "University Scene" column.

University VLSI Conferences

Two major VLSI conferences are now being organized by universities for 1981.

Chuck Seitz of the Caltech Computer Science Department is organizing a VLSI conference to be held at Caltech on January 19-21, 1981. The first VLSI conference (also organized by Chuck) was held at Caltech in January, 1979. That conference was a great success; lots of new work was reported, and an excellent proceedings published. I'm sure that many folks are looking forward to revisiting Caltech next January.

The University of Edinburgh is organizing the first International VLSI Conference, to be held in Edinburgh on August 18-21, 1981. Edinburgh University has been active in microelectronic design and design-aids research for over 10 years, has worldwide contacts in this field, and is a key participant in the new U.K. university initiative in microelectronics design. The conference is timed so that you can also attend the Edinburgh Festival, and promises to be an exciting event!

If you have university news to report, or would like to contribute short descriptions or photographs of activities at your school, we'd like to hear from you. Write to us at: The University Scene, **LAMBDA** Magazine, P.O. Box 50503, Palo Alto, CA 94303.