CARVER MEAD'S LSI COURSE @ PARC

JULY 7, 8, 9 1976

JULY 7

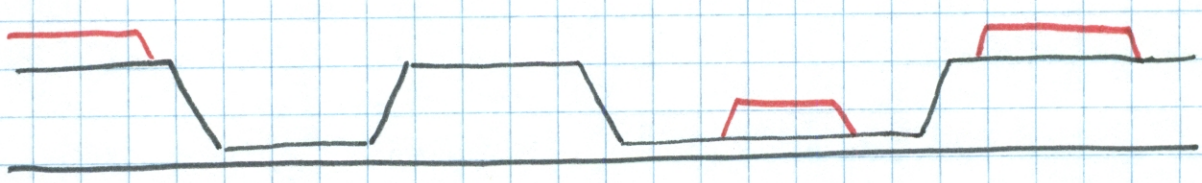
N-CHANNEL : P-TYPE SUBSTRATE

ETCH DIFFUSION WELLS, (MASK 1)

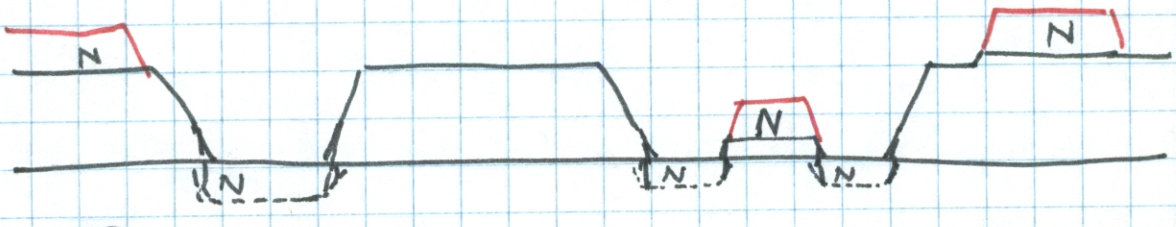
ADD THIN LAYER OF OXIDE, ~1000 Å

" " " " POLY-Si ~3000 Å

AFTER ETCH OF POLY: (MASK 2)



AFTER ETCH OXIDE : THEN IMPLANT Phosphorus IONS to form N-Type Regions

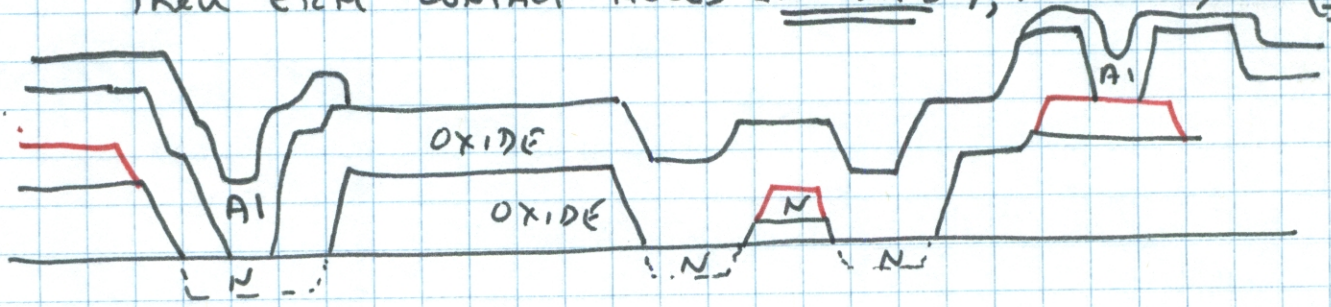


P-TYPE SUBSTRATE

NOTE: ION IMPLANTATION REDUCES UNDERCUTTING.

ADD LAYER OF DEPOSITED OXIDE ~1-2 μ

Then ETCH CONTACT HOLES (MASK 3), Add metal, Etch (MASK 4)



NOTE: BRING GATE CONTACTS UP TO POLY ON TOP OF THICK OXIDE LAYER, TO PREVENT PROBLEMS OF SOLUTION OF GATE SILICON INTO AL.

PRODUCTION: NORMAL PROCESS

FINALLY, OVERLAY WITH GLASS, ETCH CONTACT PADS (MASK 5)

GLASS CONTAINING Phosphorus IONS to prevent

production

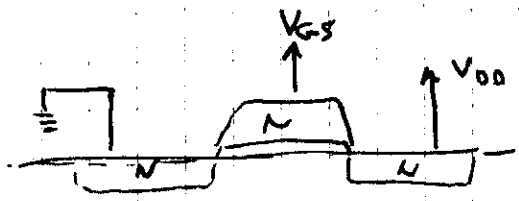
CARVER'S: PRODUCE SOME TRANSISTORS WHICH ARE NORMALLY ON (DEPL. MODE). SO ANOTHER MASK IN EARLY PART OF THE PROCESS.

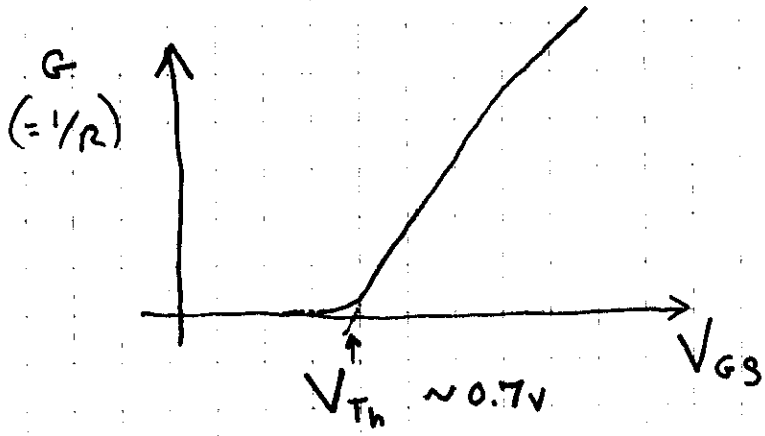
3 LEVELS OF CONDUCTOR.

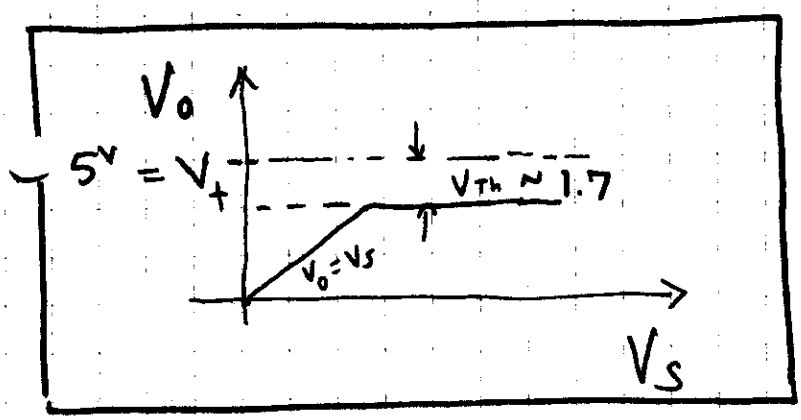
BUT CAN'T CROSS LVL 1 + 2 BECAUSE MAKES A TRANSISTOR.

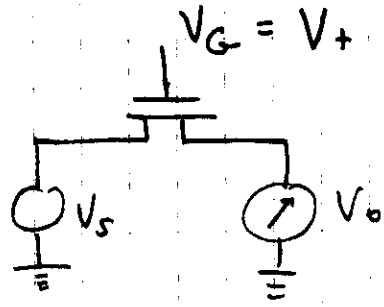
SO HAVE 2/3 OF RISK OF 3 LEVELS.

TRANSISTORS: ENHANCEMENT MODE:









The threshold is a function of V_S Because of effect of substrate:

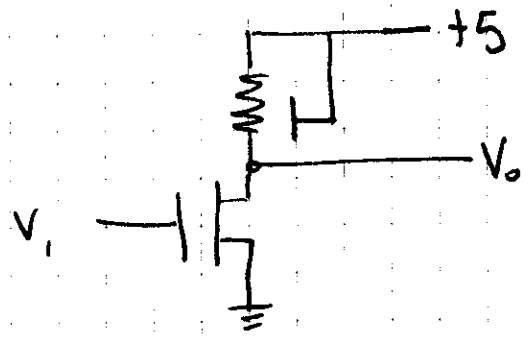
i.e.: $V_S = 0 \Rightarrow V_{Th} \sim 0.7$

$V_S = 3V \Rightarrow V_{Th} \sim 1.7$

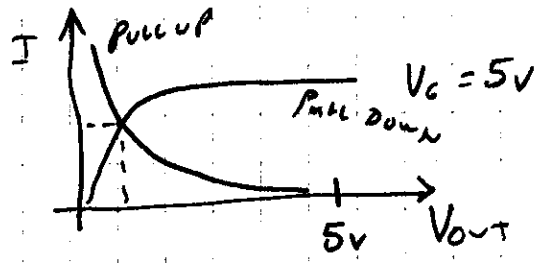
↓ V_{Th} increases with increasing V_S.

Now: Resistance of Transistor when on, if □, ≈ 10KΩ

while resistance of the various conducting elements is low. So use Trans. for resistors.

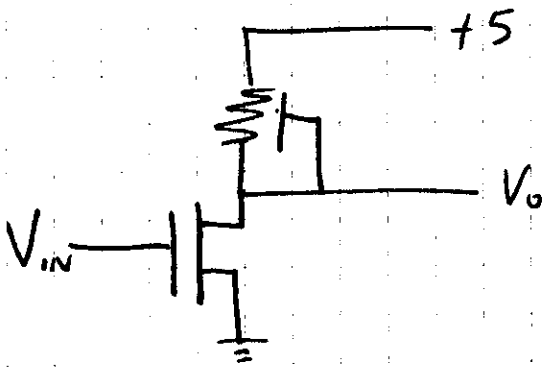


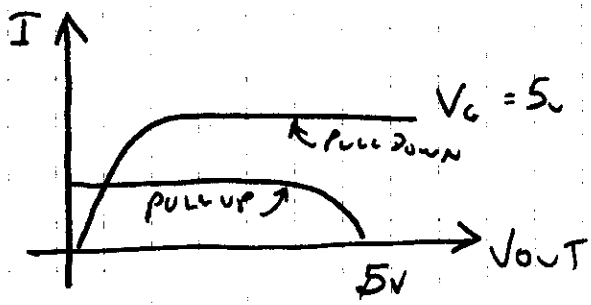
This, using Enhancement mode MOSFET for R is bad because:



So: Lose drive as try to bring V_o back up and high current needed to bring V_o down.

Alternative: use depletion mode MOSFET for the load R: (normally on)

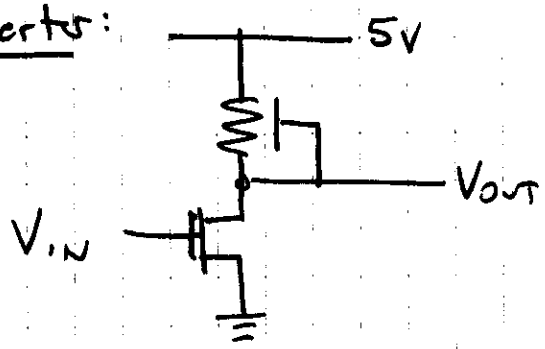


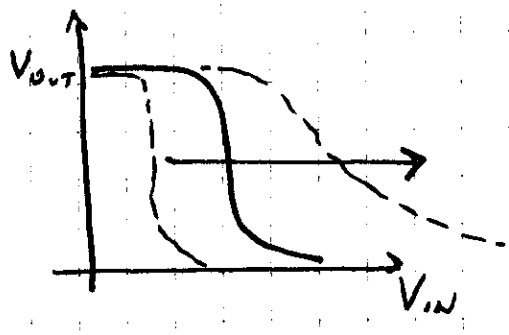


MORE CURRENT FOR DRIVE, LESS CURRENT FOR BRING DOWN. MUCH FASTER FOR GIVEN PWR.

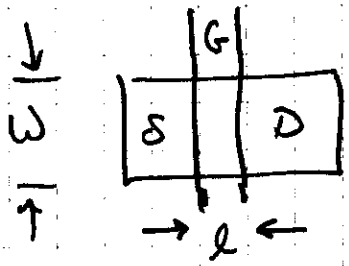
TO DO: ANOTHER MASK SELECTS SOME OF THE IMPLANT WELLS FOR SLIGHT CHANGE OF DOPING TO CHANGE THRESHOLD OF SELECTED TRANSISTORS.

The Inverter:

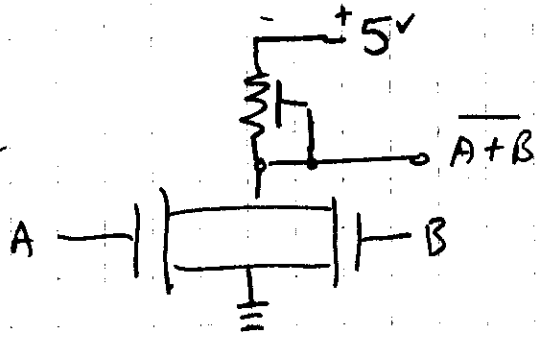


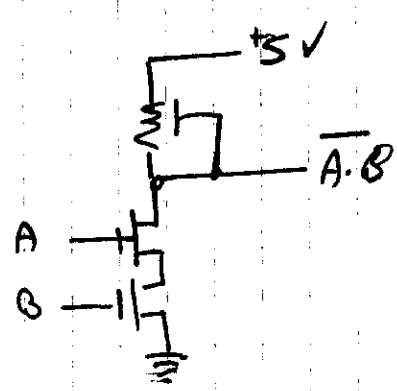


arrow shows effect of decreasing the relative "length" of the load T with respect to the inverter T.



Refer to "length" as ratio l/w.

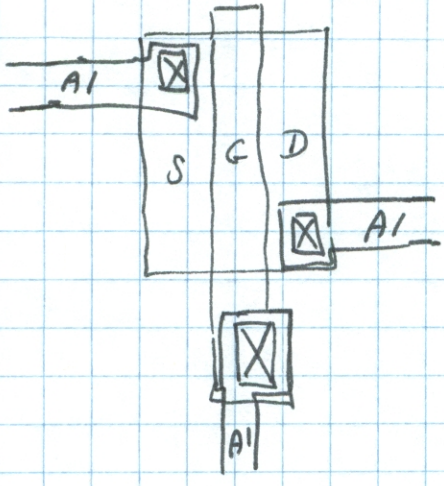




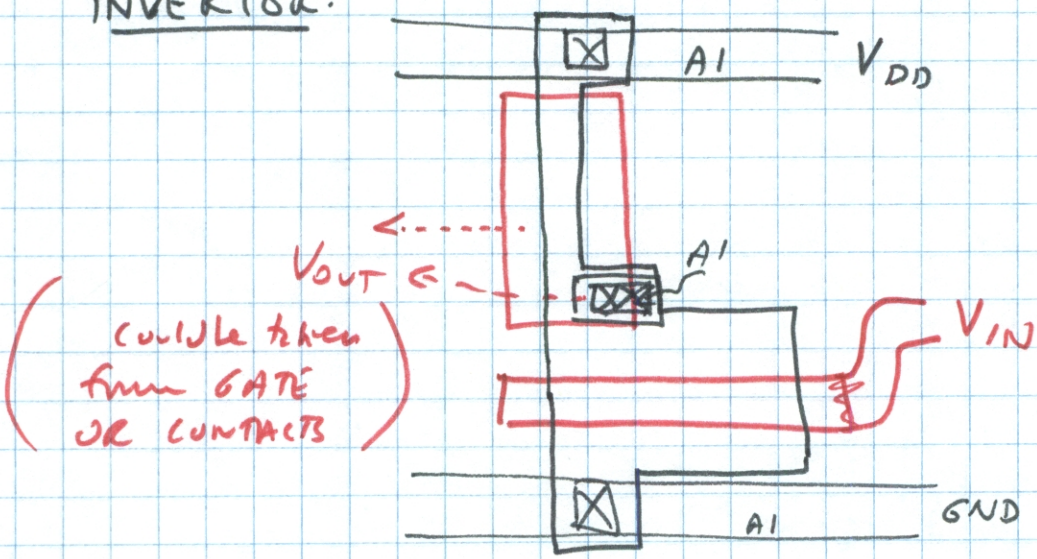
The load T here will have to be "longer".

Develop Design Rules, etc:

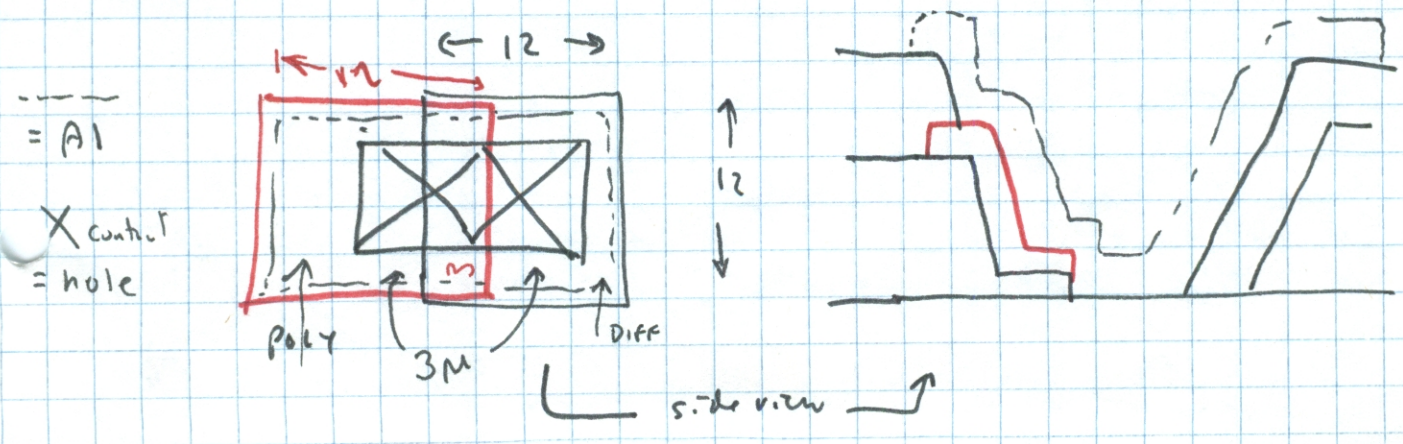
First: Make A Transistor:



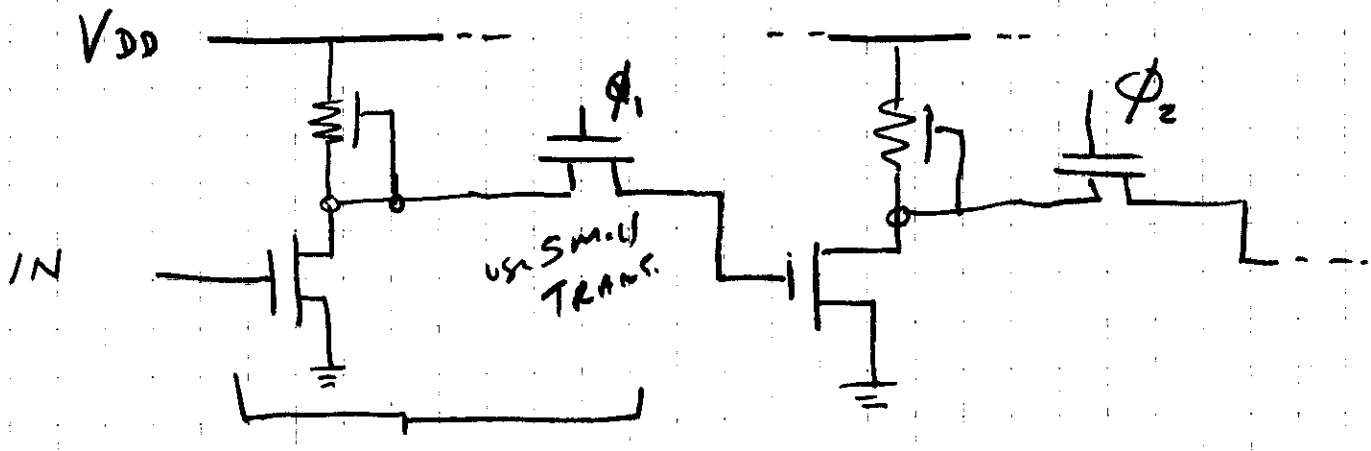
INVERTOR:



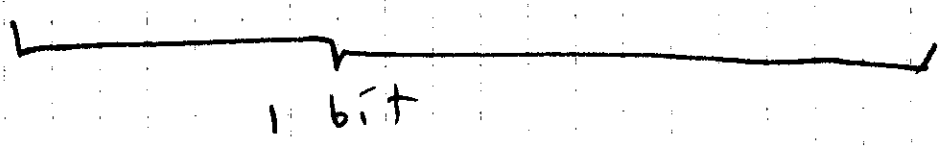
Some Rules: See Notes: Detail on contact between Gate & Diffusion

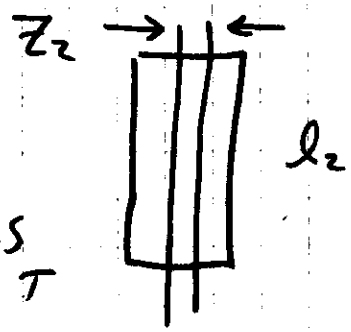


Shift Register: Dynamic using storage of charge on gates:

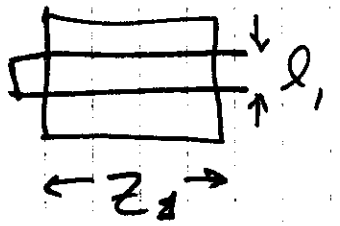


3 Transistors per 1/2 b.f.





~ Res LOAD T



INV. T

z_2/l_2 = drain c.p of pullup

z_1/l_1

$$\frac{\frac{z_1}{l_1}}{\frac{z_2}{l_2}} \cong 4$$

for threshold of $\approx 2^V$

DESIGN SHIFT REG CHIP:

1. V_{DD} + GND IN METAL

2. Design one cell that can be repeated, noting that row below data goes in reverse direction.

3. V_{DD} + GND should alternate (not both for each row).

4. So: Design six through cell that repeats in X, Y.

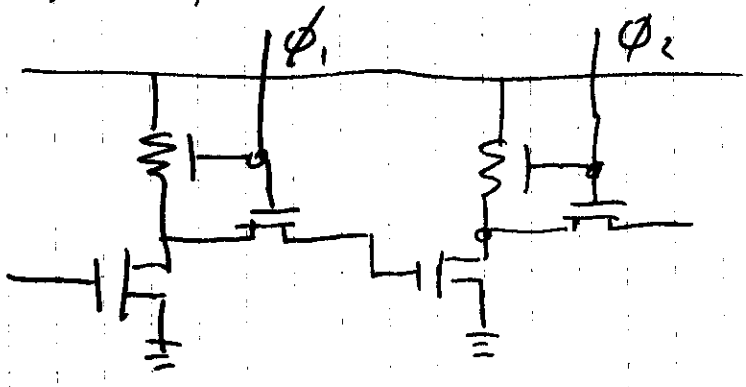
5. AN exceptional Design would be 80×100 for full 16-bit with old rules with metal for clocks.

   Using red for clocks + new design rules, then should get ≈ 40×40 for 1/2 bit.

   No: feed thru on depl. T adds to space.

   Maybe ≈ 60×80 or so.

Could design using enhancement mode LOADS



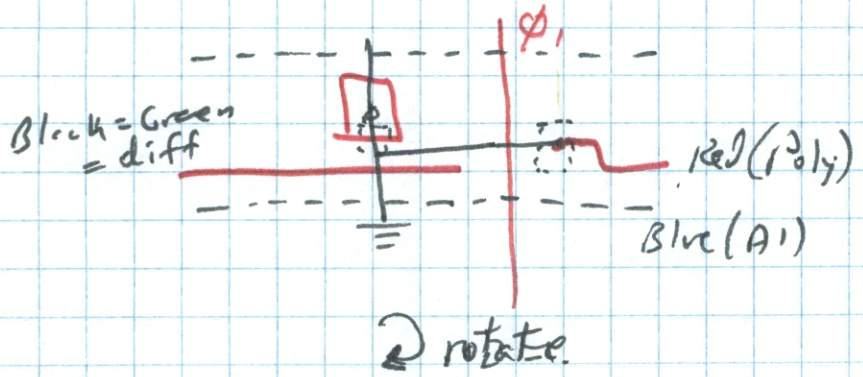
, etc.

Use 10x10 to 1/2" graph paper.

Where each square is a micron.

Do the depletion mode case.

START WITH "STICKMAN" (FORGETTING RULES)



2 rotate

(1) SiO_2

Si

(2) ~1010Å

Diffusion MASK 1 expose etch

then Gate oxidation

(3)

Poly-Si: Si_3N_4 Non Amor. Si

(4) B

P P

Channel Mask 2 xpsr etch

then diffusion

(5)

SiO_2

(6)

Contact hole MASK 3 exp etch

(7) metal overlay

(8) Al

Metal interconnect Mask 4

(9)

SiO_2 overlay

(10)

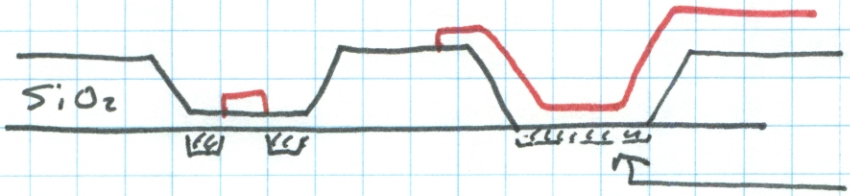
MASK 5 contact pads

THE BURIED CONTACT:

Note:

Note: use of xtra step to make a

POLY-Si to Substrate connection:



remove thin oxide by xtra Mask Step.

Diffusion is less than 2μ but does occur.

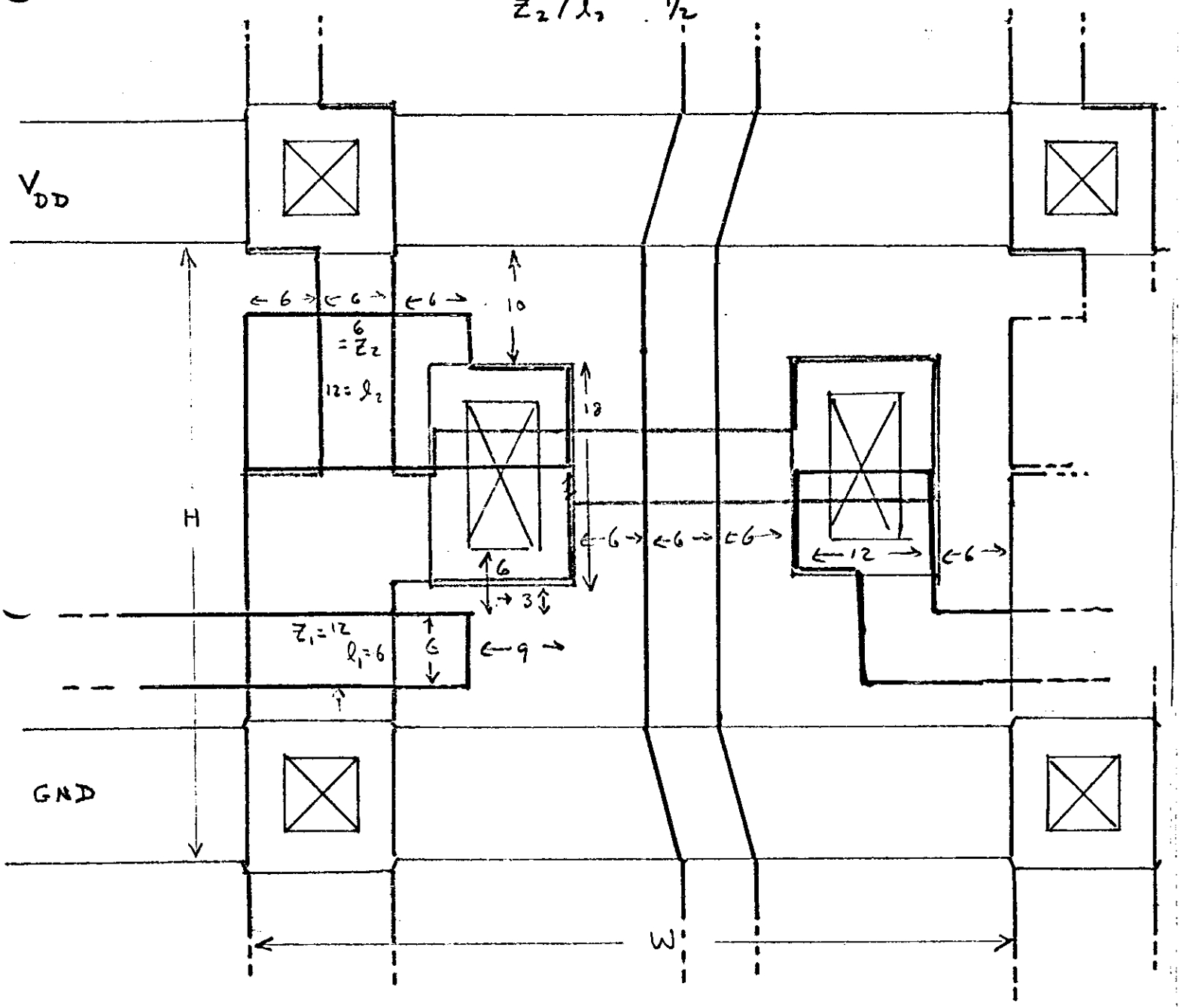
PROBLEMS: GROWTH OF DENDRITIC SPIKES AT JUNCTION OF SINGLE CRYS. GROWTH & POLY

CARVER SAYS THAT THIS STEP REDUCES YIELD AND ISN'T REALLY GOOD IN GENERAL.

DYN. SHIFT REGISTER 1/2 BIT CELL: 1 SQ = 3μ

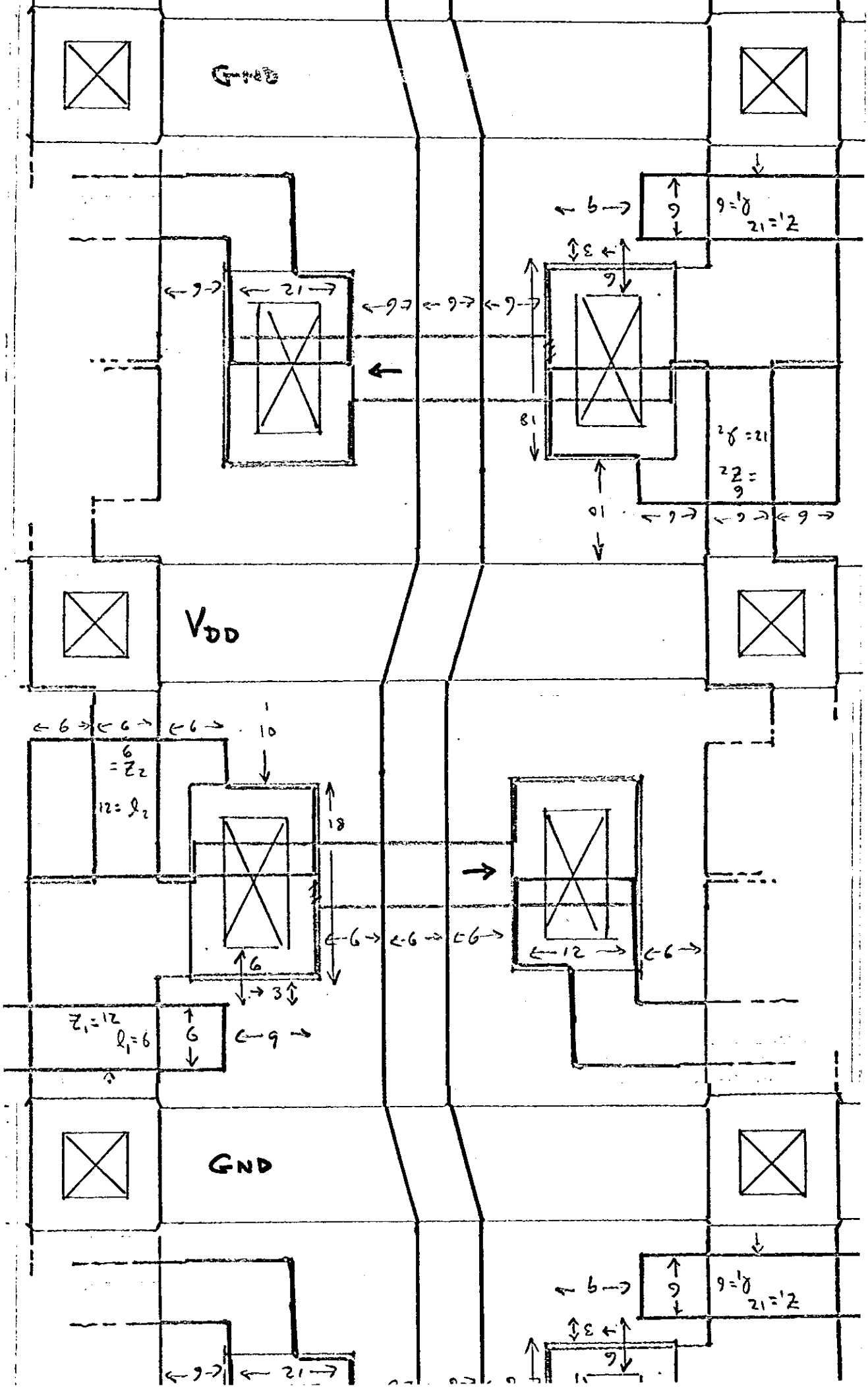
(Rotate for Reverse Direction Rows) L. Conway

$$\frac{Z_1/l_1}{Z_2/l_2} = \frac{2}{1/2} = 4$$

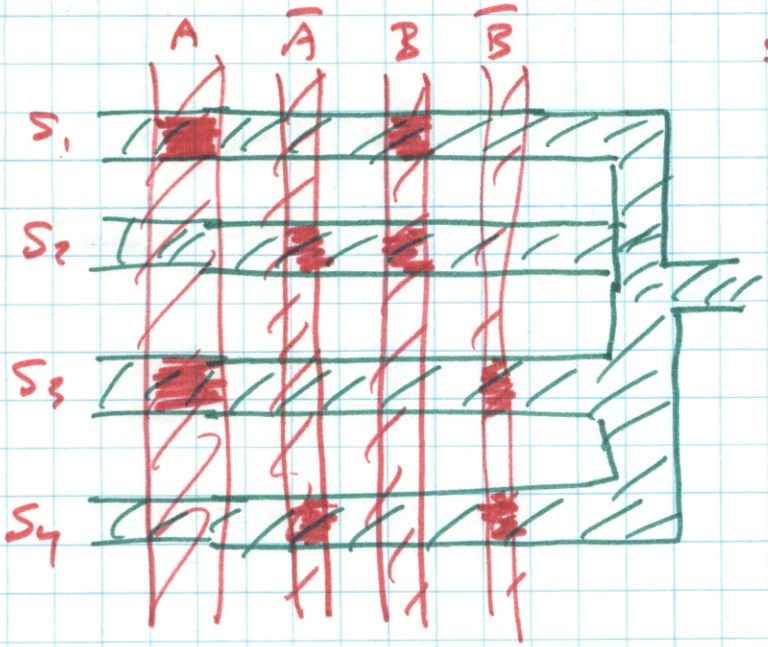


H = 10 + 18 + 3 + 6 + 6 + 6 + 3 = 52 μ

W = 18 + 9 + 18 + 12 + 6 = 63 μ


GND
VDD
GND

EXAMPLE: IN AN ALU



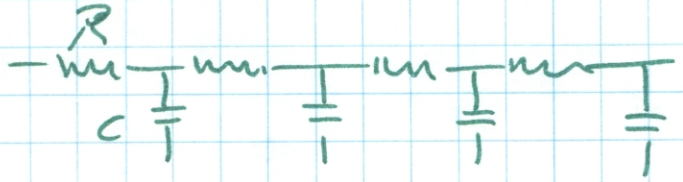
SOLID RED → DEPL MODE

$S_1 \cdot \bar{A} \cdot \bar{B} + S_2 A \cdot \bar{B} + S_3 \bar{A} \cdot B + S_4 A \cdot B$

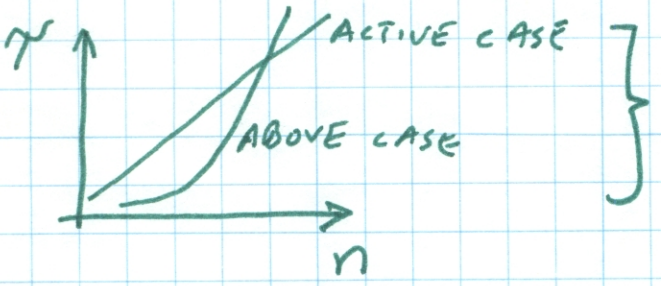
(only use to feed gate)

This is approach IVAN p-shiz: note lack of feedthrus & "no" power req'd.
(Manchester chain)

Note: Time delay $\cong RC\,n^2$ (n = # RC lines; delay for pulse edge)



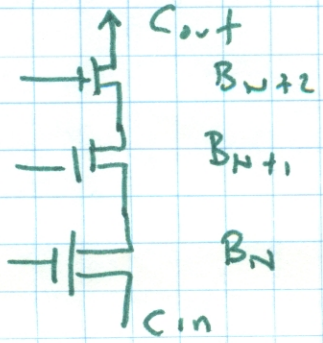
R: pull-up T resistance
C: assoc cap.



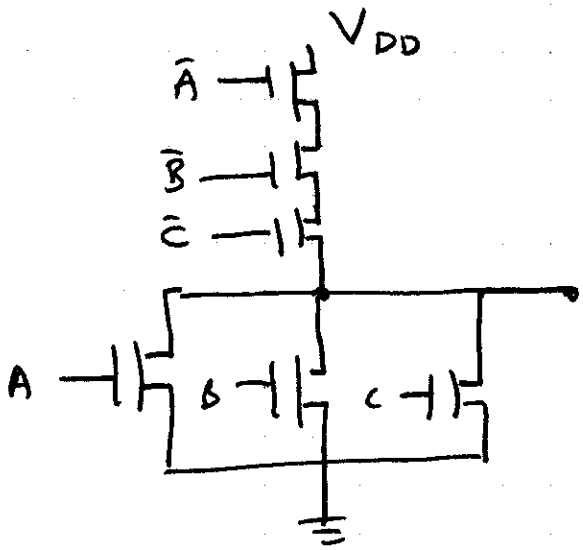
for small n, the above approach is actually faster

EXAMPLE OF APPLIC: CARRY PROP. IN ADDER:

How to minimize delay? →



NOTE: IF DOUBLE RAIL INPUTS AVAIL } IVAN'S IDEA FOR POWERLESS LOGIC.



NAND or NOR
DEP. ON VDD/GND REVERSAL

To level restoration

ALL N-Channel Devices.

IN C-MOS WOULD HAVE SAME DIAGRAM, BUT THE SERIES T's WOULD BE P-TYPE, PARALLEL WOULD BE N-TYPE, ALL INPUTS UNCOMPLEMENTED.

use 4 bits of carry produced by Manchester chain, then restore with inverter.

NOW: SUPPOSE WANT OUTPUT OF CHAIN SOMEWHERE ELSE:

COULD RUN WIRE: BUT CAPACITANCE WOULD BE HIGH + RES. OF DRIVER HIGH — VERY SLOW.

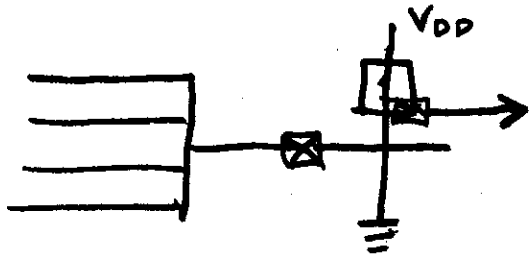
FACTS: ① CAP OF GATE TO CHANNEL

$= 3.5 \times 10^{-4}$ pf/μ^2

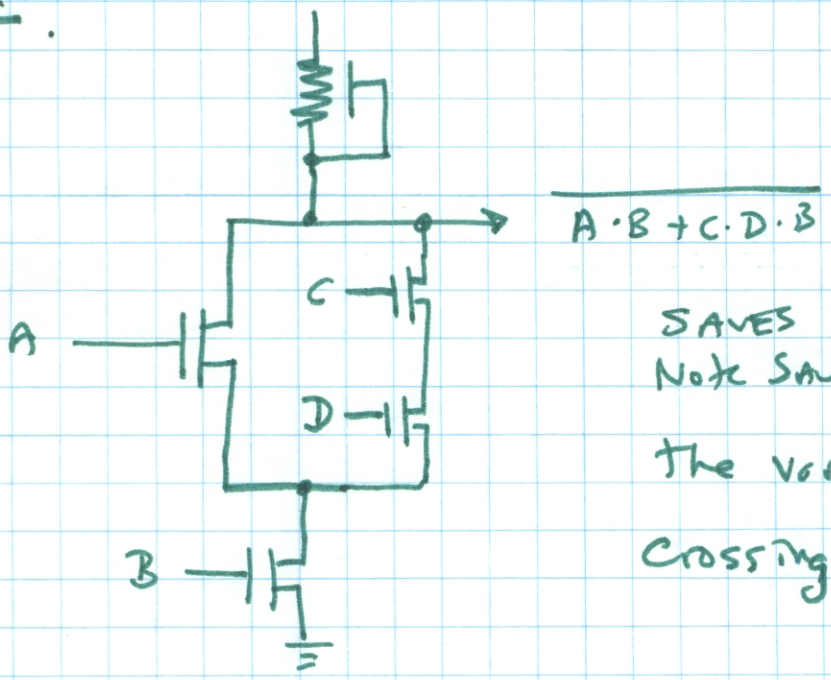
② Diff $= 0.35 \times 10^{-4}$ pf/μ^2

③ Metal $= 0.2 \times 10^{-4}$ pf/μ^2

TO SPEED UP MANCH CHAIN USE INVERTER.

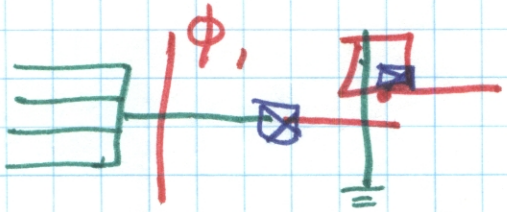


EX:



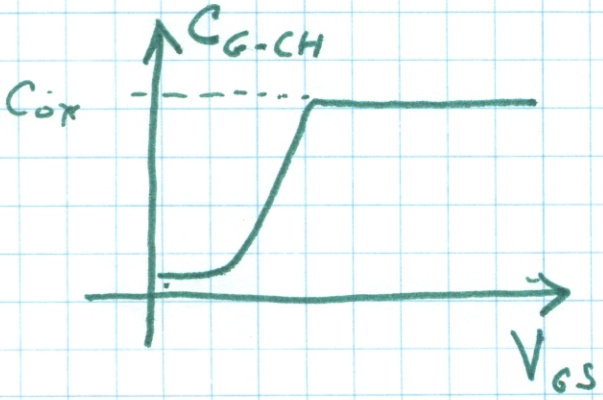
SAVES PROPOG. DELAYS, POWER,
NOTE SAVING OF PULL-UPS;
the various T's are just
crossings of +

NOTE: use of clocks prior to latching. Normally 2ϕ.
Elim. need for cross-coupled memory elements.

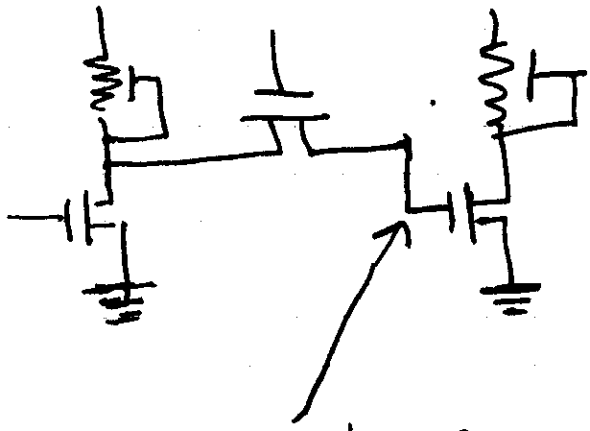


, etc.

NOTE: CAPACITANCE GATE TO CHANNEL IS ONLY LARGE WHEN T IS ON:



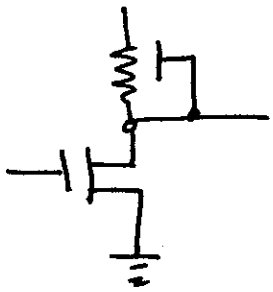
Because of this effect:



when 0 on node, cap is low. (PROBLEM).
" 1 " " , " " high

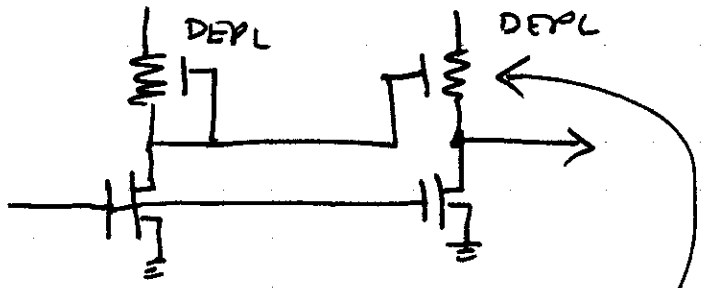
So, the case when a 0 is stored presents a problem since low capacitance for its storage.

DRIVING CIRCUITS:



OR

SUPER BUFFER:



"SMALL" INVERTER

DRIVES GATE

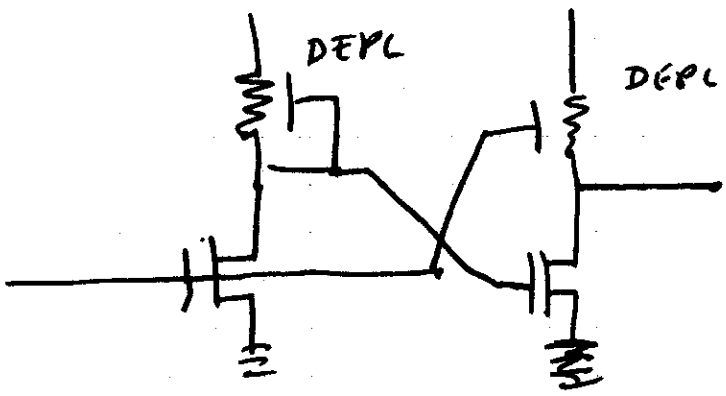
TURNED ON "MORE" THAN SAME SIZE @ LEFT

SUPERBUFFER WILL DRIVE WITH ONE SQUARE HERE.

FACTOR OF SIX IN DRIVE CAP.
" " " IN SPEED FOR PWR.

NON-INVERTING SUPERBUFFER:

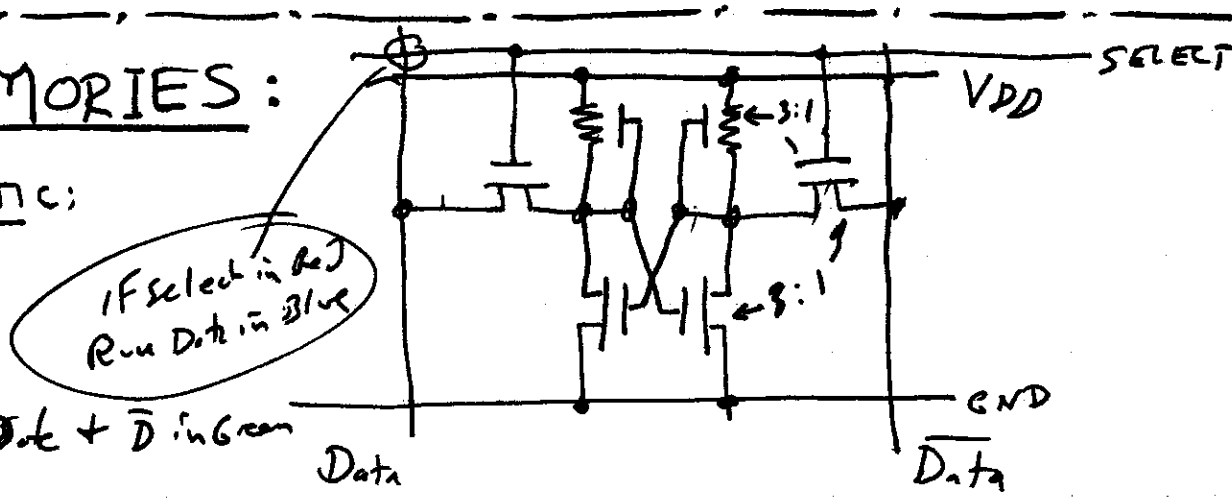
REQ 5V DRIVE
(LEVEL RESTORED INPUT)



SMALL PULLUP R WHEN WANT TO PULL-UP, LARGER " R WHEN " " PULL-DOWN } IN BOTH CASES OF SUPERBUFFER

MEMORIES:

STATIC:



OR: Run Data + $\overline{D}$ in Green

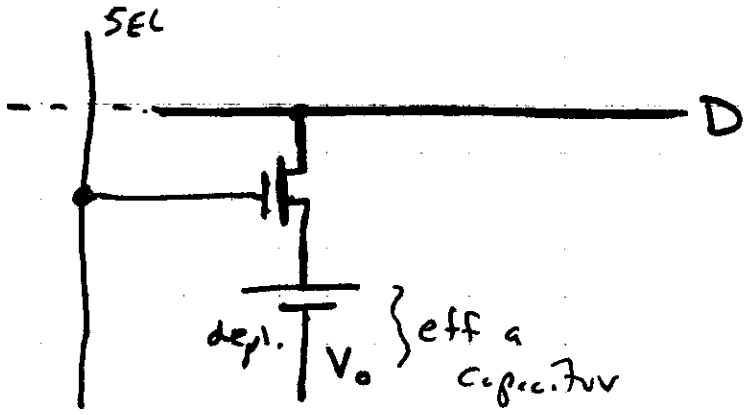
Do this tonight: use 3:1, 3:1 as the $\frac{Z/c}{Z/c}$ ratios

Do not use buried contact.

Run at least GND in metal. Maybe little in Green

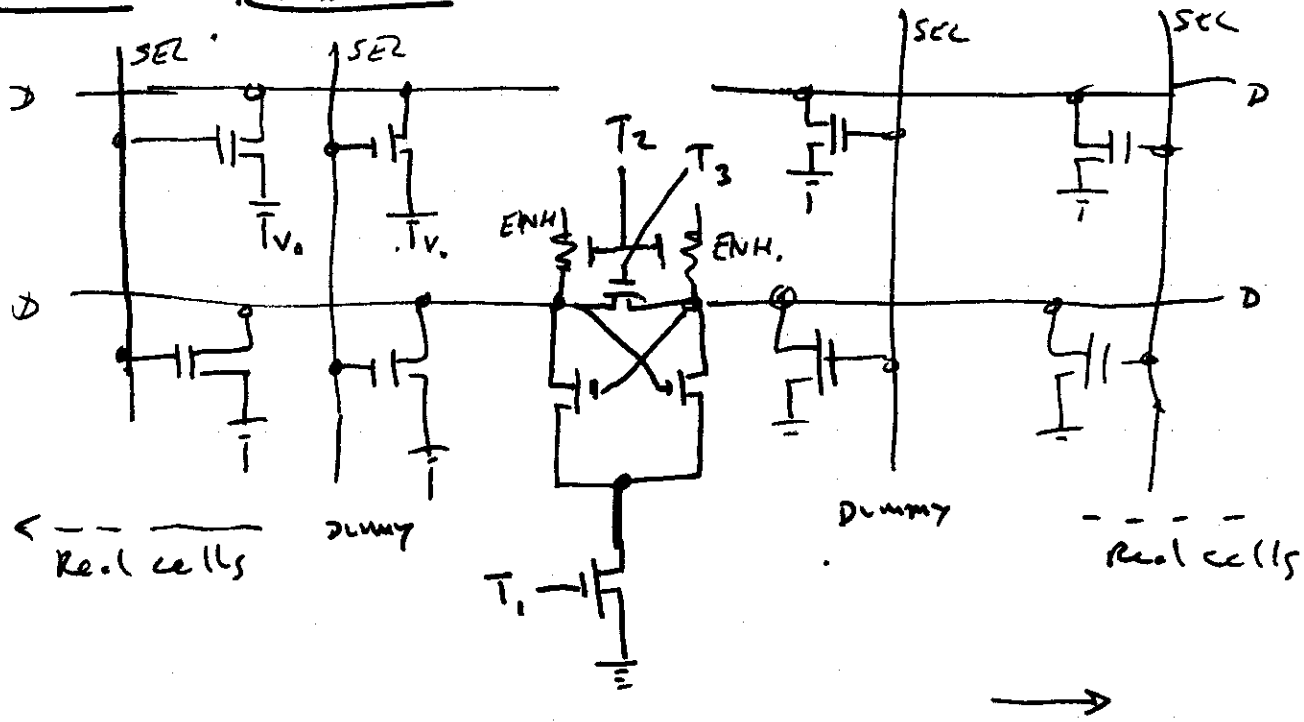
Could run V_{DD} in Green for a while.

DYNAMIC MEMORIES:

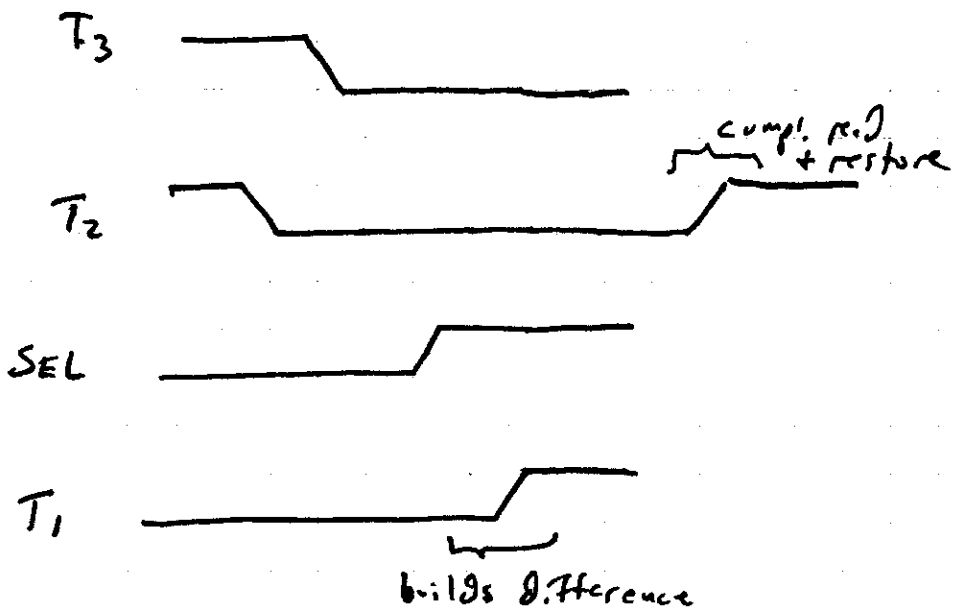


TO WRITE: Put D on, hit select. Charges C to 1 if D=1. Disch. to 0 if D=0. Then unselect.
Slow leakage to substrate.
Refresh in ~ 1 MS.

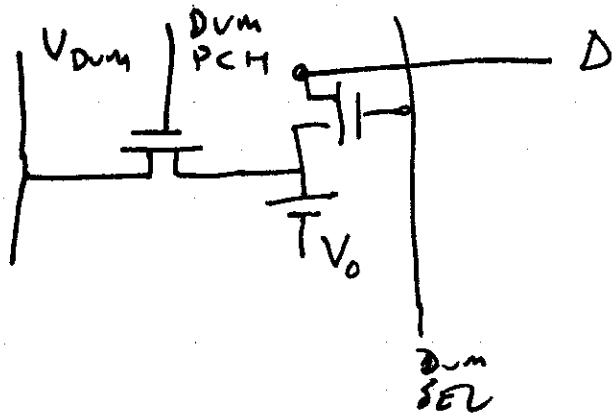
TO READ: By Differences: USE BANK OF DUMMY CELLS:



To Read: (cont) Manipulate T_i's as follows:

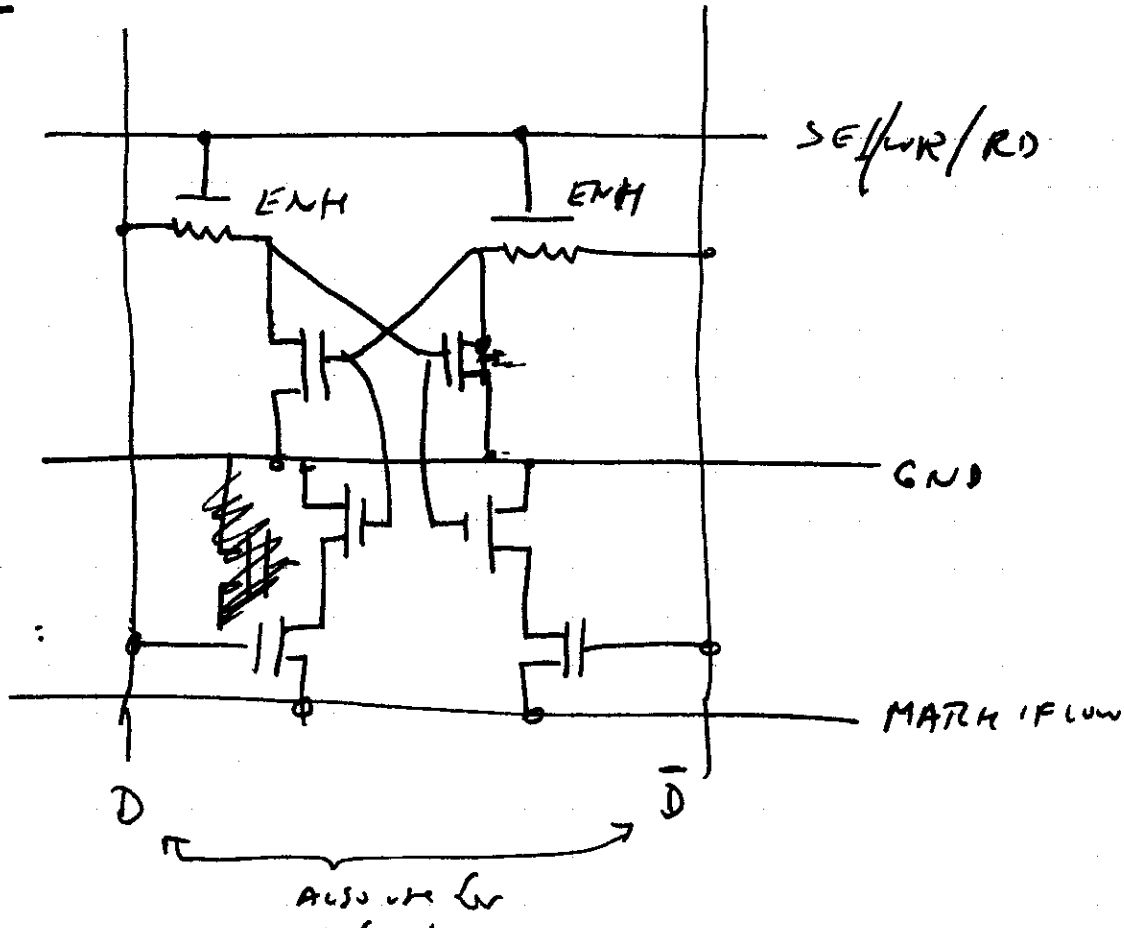


Note: Precharge of Dummies by another input of transistor, as:



This is technique used to implement the current large chips from INTEL, etc., according to Carver.

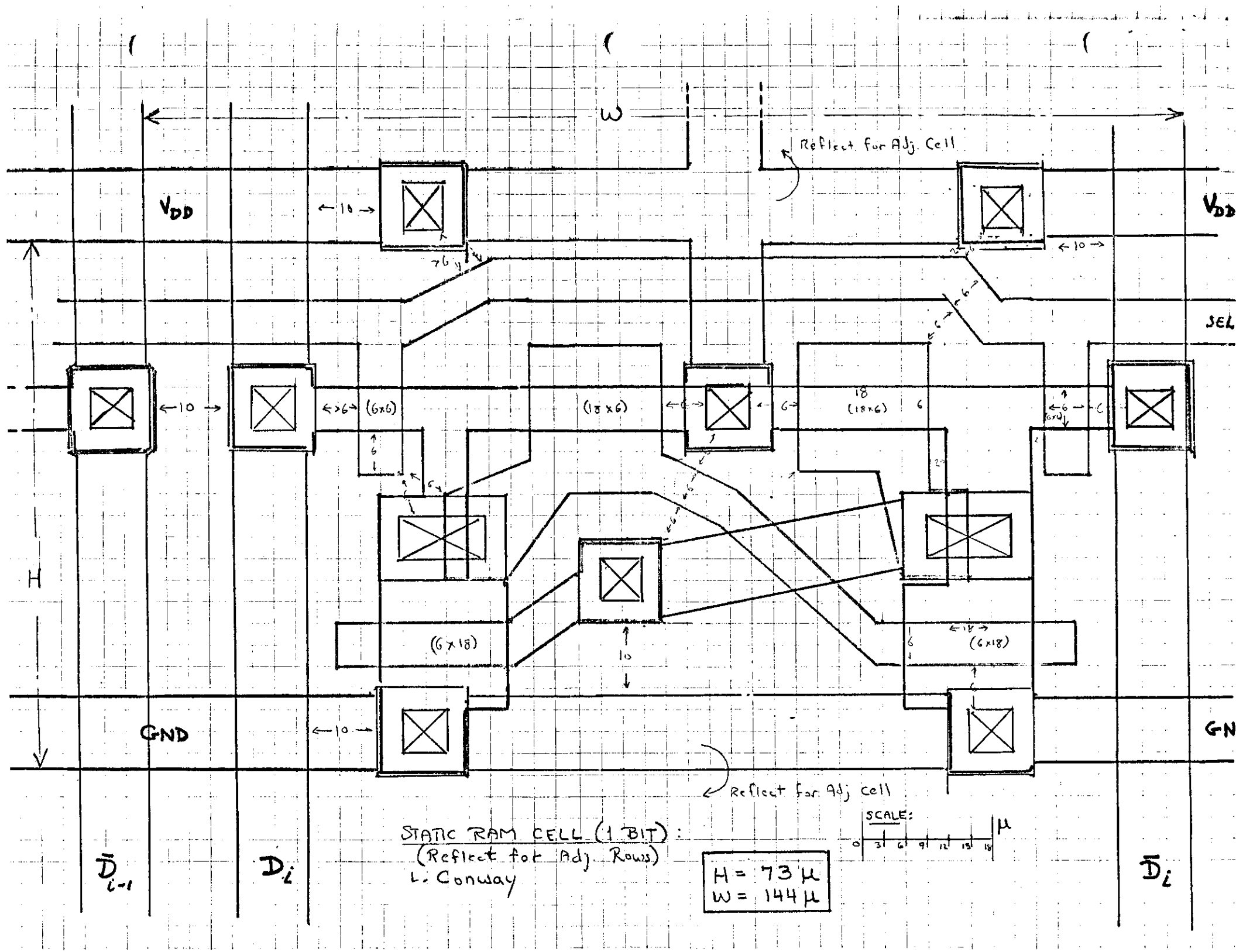
CAM:



MOSTLY STATIC,

BUT DYNAMIC WHILE DOING MATH.

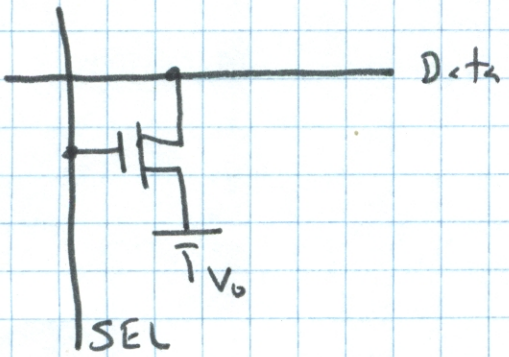
IF COMP FN TOO LONG, CHARGE GOES AWAY.



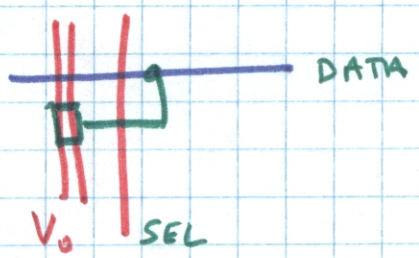
STATIC RAM CELL (1 BIT):
(Reflect for Adj. Rows)
L. Conway

H = 73 μ
W = 144 μ

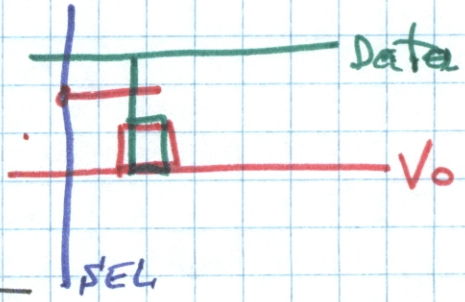
TO IMPLEMENT:



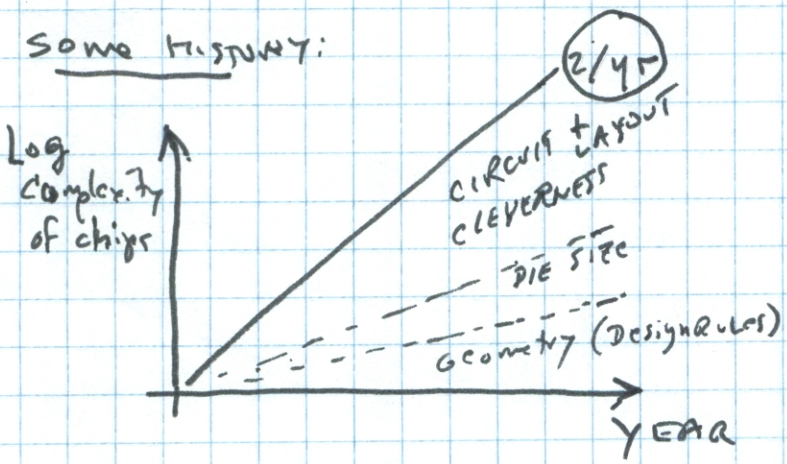
(a)



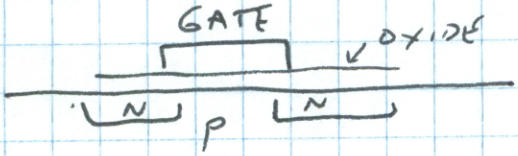
(b)



SOME HISTORY:



SCALING: OF THE TRANSISTOR:



suppose scale everything incl. oxide thickness by factor k:

$V \sim k$; $C \sim \frac{k^2}{k} = k$ ← due to thickness

$G \sim$ const.

$\therefore$ Time Const $\tau \sim k$

$PWR \sim K^2$

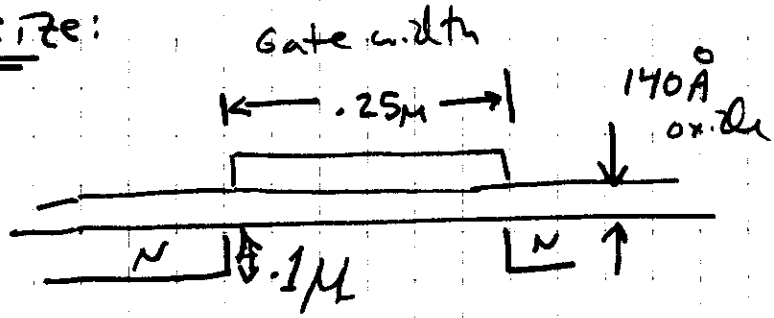
SCALING (CONT.)

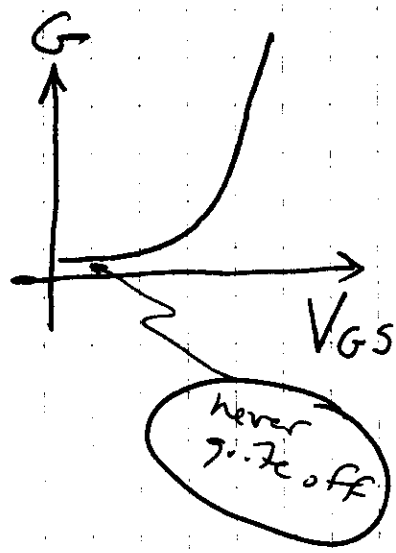
So PWR per unit area $\cong$ const
with $\tau \sim k$ and #/unit area $\sim k^{-2}$

$\therefore$ every reason to make smaller Transistors.

What are the physical limits: AN EXAMPLE:

for size:

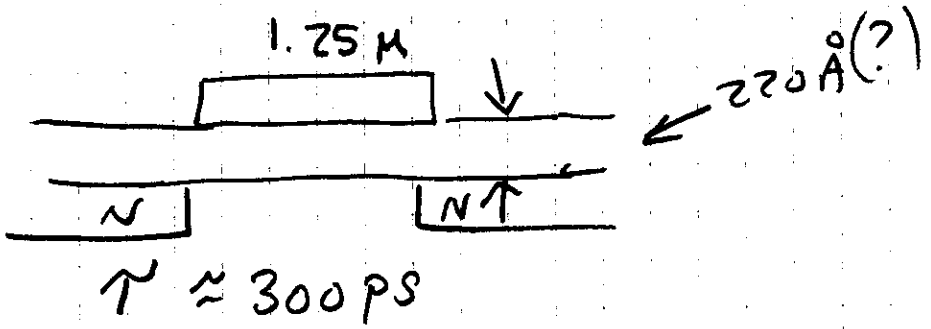




for this size: $V_{applied} \cong 1^V$

$V_{Th} \cong .25^V$

IBM YORKTOWN: SAYS SMALLEST T they have made:



$\tau \cong 300$ PS

What Might Process Look Like:

Problem of Back Scattering of E-beam.

Intermediate Mask made by E-beam. (Not used on) onto Mylar. Deposit Gold, silicon

Use Soft X-rays (~100 V) onto photo resist. to actually expose/etch chip.

Need highly collimated, intense beam.

As get further away, collimation better. but intensity is low

Problem of exposure-time.

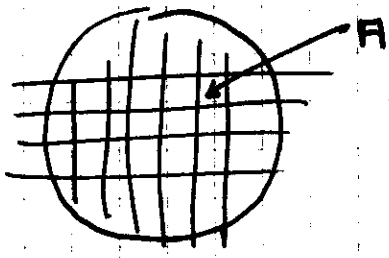
Use Polygon Synchr. Ring
Synch. R.D. at bends.

Problem Remains: Alignment → chip by chip

RATIO: $10^5/1$ now ~ limit on resolution within a wafer

Defects: **N Defects/cm² ~ Random:**

∴ Yield in Good Dic/wafer $\sim \frac{1}{A^2}$



Note: ∴ yield scales as $\sim \frac{1}{k^4}$

However: Defects aren't really random, so effect is less severe.

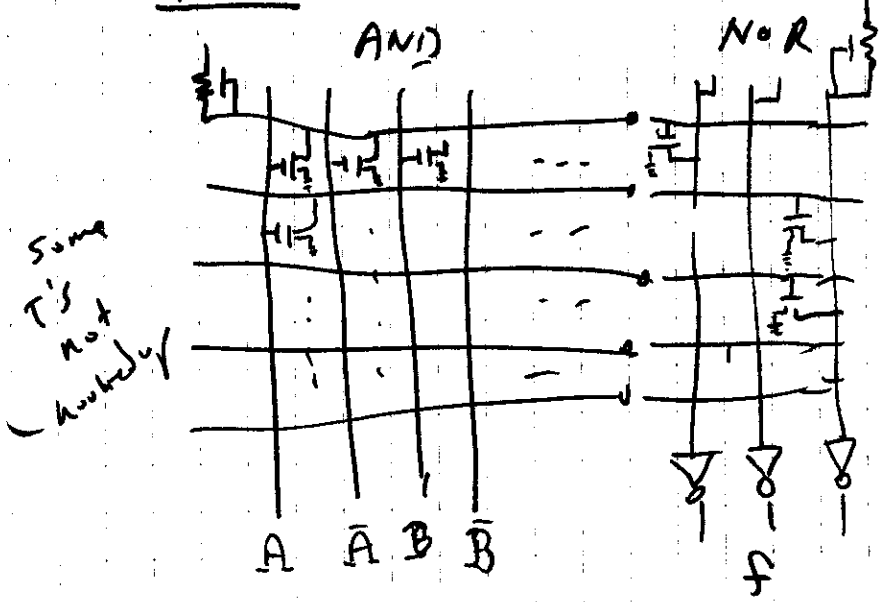
[N is now: yield ~ 10% @ 200 mils (?)]

LARGE CIRCUITS:

Since distance + # wires both go as N (# of nodes), then fraction of area devoted to wires goes as N.

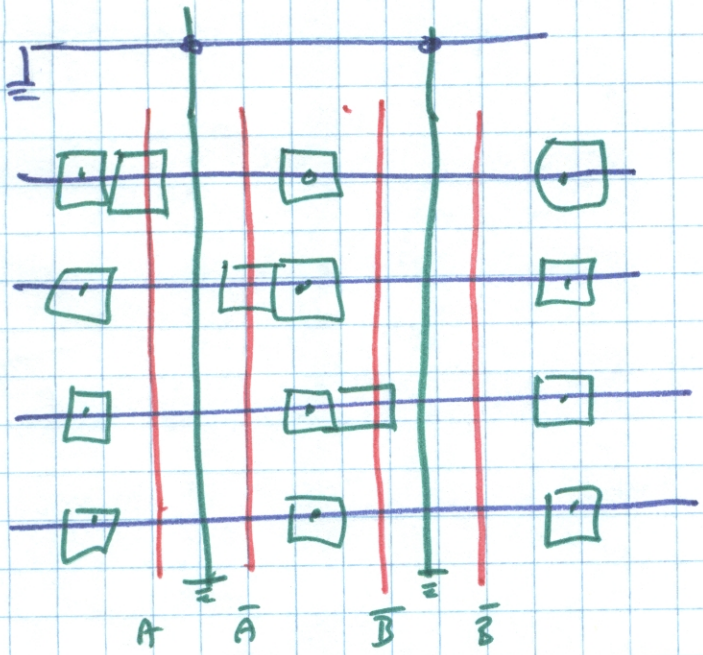
So— in large chips, use regular structures.

EXAMPLE: PLA:



Layout:

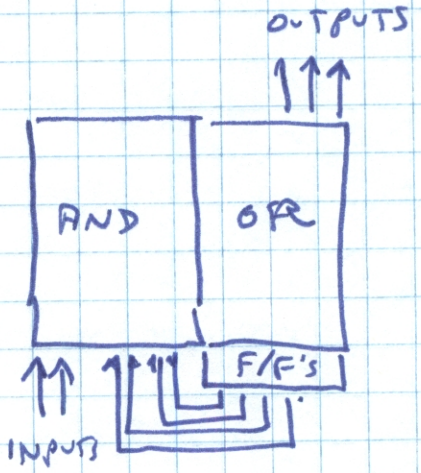
PLA LAYOUT:



tilt over for the NOR

PROGRAM AND BY
ADDing Green SQ over Red
Each cell is ~ 20x20M

SO: IN APPLIC:



EX: OF PLA USE: EX OF SMALL AMT OF REAL ESTATE DOING "RANDOM THINGS"

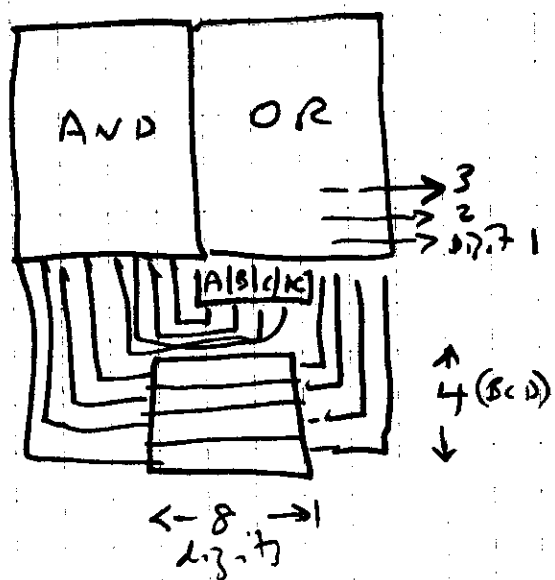
BUILD A CLOCK: START WITH 60 CYC:

$\div 6, \div 10, \div 6, \div 10, \div 6, \div 10, \div 12,$

BCD → 7 BAR DECODER, MULTIPLEXER, ...

TYPICALLY NOW: (MOSTEK etc) 180 mil chip.

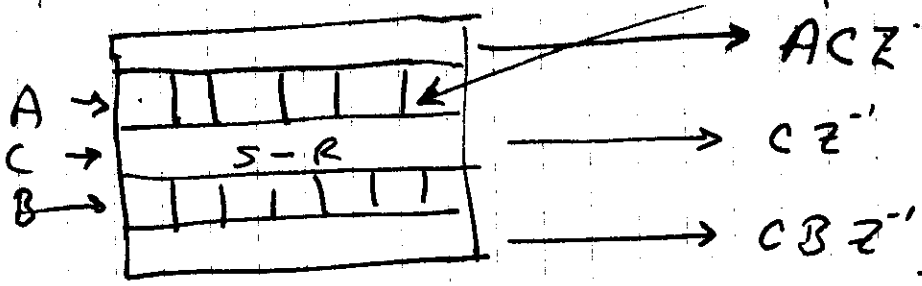
STATES: A, B, C, K
which DIGIT



Phaselock to LINE to clock this.

This chip (with old rules) [Equates 14 MHz OSC]
110 x 68 incl. drivers, etc.

MULTIPLIER EXAMPLE:



PRODUCES CANONICAL DIC FILTERS =