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January 5, 1979

To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #6**

Filed on [MAXC]<Conway>MPC79.memo6

The MPC79 implementation has been successfully completed! The chip-set includes 82 VLSI design projects from 124 designers. The implementation turnaround time for MPC79 was 29 days. (from design files to distribution of packaged chips).

Packages containing the project chips were distributed on January 2, 1980. On January 2 the packages were hand delivered to Caltech, Stanford, and U.C.Berkeley, and were mailed special delivery to instructors or coordinators at M.I.T., CMU, Univ. of Rochester, Univ. of Illinois, and the Univ. of Washington. Packages were mailed to individual designers at Univ. of Colorado and Univ. of Bristol the following day. All coordinators should have received the shipments by now. It's likely that most of the chips will be distributed to the student designers during the next few days, just as the new semester begins at most of the schools.

This message (i) provides information about the implementation activities during the past 4 weeks, (ii) describes what the MPC79 shipments contain, and (iii) describes some things that coordinators should do before distributing the chips and their documentation. It also discusses our plans for further documentation concerning MPC79, and our interest in receiving feedback from the designers, to include in that documentation.

If you have any questions or wish to provide testing results or other feedback, you can continue to reach us via MSGs to MPC79@PARC-MAXC.

THE EVENTS SINCE DECEMBER 4:

The events of the past four weeks since the design cutoff time of 5:00pm Tuesday December 4 have been as follows:

We started final processing of the implementation REQUESTs immediately following the design cutoff time. This processing continued on into the evening. During the night of 4-5 December we operated the MPC implementation system to plan and effect the merging of the projects into the various MPC79 chip-types, and to then convert the merged CIF files into MEBES format files. At 10:00 am the next morning we took the merged mask-specification data to Micro Mask.

Delivery of the masks was pipelined with the early fabrication steps, with the first mask of both mask sets being delivered at 5:00 pm, Thursday Dec. 6. By then, HP-ICPL had already started the

processing and were ready for the first masks. Processing continued normally except for one major contingency: the failure of a poly-deposition system (causing a delay of about 8 days for repairs, and leading to an additional delay in wafer processing due to the Christmas holidays). At 10:00 am on Dec. 28, the type-B wafers completed fabrication. The ring oscillator test structures were probed and found to work. One project, Jim Clark's system-clock, was bonded and tested on the afternoon of Dec. 28, and was found to work completely. On Monday Dec. 31 the type-A wafers completed fabrication, and were found to be satisfactory. Packaging, bonding, document generation, and document printing proceeded through January 1. The shipments were mailed at 5:00 pm, January 2.

WHAT THE SHIPMENTS CONTAIN:

The shipment to each university contains (i) a collection of boxed, wire-bonded, packaged chips for that group of designers, (ii) a set of wire-bonding maps for those chips, marked-up to show the custom wire-bonding of each project, (iii) copies of the "MPC79 Implementation Documentation" to be distributed to all designers, and (iv) a questionnaire and return envelope for the designers, so that you all can provide us with some feedback. Coordinators should check to make sure that all this stuff is included in their school's shipment. This shipment provides each project coordinator with ONE packaged, wire-bonded chip for each PROJECT, and ONE set of documentation for each DESIGNER and for each STUDENT in the design course (including those who did not complete a design).

[Some unpackaged chips are also included in certain shipments. These can be packaged by the universities, and used by designers who need a second copy if they suspect that their first copy has manufacturing defects. We'll provide additional unpackaged chips later on. We can provide some additional packaged wire-bonded chips on request (depending on demand and timing); we'll expedite further packaging for those designers who are seriously testing their projects.]

DISTRIBUTING THE CHIPS AND DOCUMENTS:

Coordinators should carefully read Sections 2, 3, and 7 of the "MPC79 Implemention Documentation" before distributing the chips and the documentation to the designers.

Each boxed, packaged chip is marked with a code number. SECTION 2 of the Implementation Documentation describes how to associate these code numbers with the project ID's, so you can figure out which box belongs to which designers(s). SECTION 2 of the documentation also provides important warnings and tips about how to handle the chips and how to prepare them for testing. PLEASE request that designers READ SECTION 2 of the Implementation Documentation before doing anything with their boxed chips.

TESTING:

It is now up to you coordinators and designers to get those projects tested! Be sure to let us know how things went. We'd like to know which projects worked, and which ones didn't. Of the ones

that had bugs, we are very interested in the nature of the bugs, and also whether, and how, you figured out what went wrong. A short one-page questionnaire and a return envelope have been included for each student in the shipments. You can use these to send in your detailed test results. Try to get as many questionnaires back to us as possible before 31 January 1980. You can also send us test results by MSGs to MPC79@PARC-MAXC.

OUR PLANS FOR FURTHER DOCUMENTATION:

We are compiling a proceedings documenting the MPC79 effort, to be published as a Xerox PARC/SSL Report entitled: "Proceedings of the MPC79 Multi-University Multiproject Chip Set Project", edited by A.Bell, L.Conway, R.Lyon, M.Newell. This proceedings will include a general overview of MPC79, photos of various die types, information from the MPC79 ARPANET message traffic, information about the MPC Implementation System, and feedback from the universities.

We hope to include a collection of short-form project reports describing a number of the MPC79 projects (an example of such a report is included in the Implementation Documentation). Coordinators should especially encourage the designers of innovative projects to send us a report for the Proceedings (the deadline for reports is February 29, 1980). Designers may use the MPC79 questionnaires to let us know of their plans to submit a report.

The Proceedings will be printed in large quantities and distributed widely in the universities and in industry. We will send out copies to all participants. Instructors and coordinators: Make sure that your school is represented by some good reports in the Proceedings! For any of you designers who'd like some visibility, now's your chance!

PLANS FOR CHIP PHOTOS:

A commercial photographer will soon produce 8" x 10" photos, in color and in B/W, of each of the MPC79 die-types. We'll send some copies of these photos to each university, along with info on how to order more copies from the photographer, and how to arrange for individual project photos to be made.

LOOKING AHEAD:

Many of the MPC79 designers are already looking ahead, making plans for iterating their designs, and dreaming up more ambitious design projects. Many other university students will want access to VLSI implementation, so that they too can have the experience of learning to design in a state-of-the-art technology by actually doing it. The demand for such services may build rapidly, once folks know that it is feasible, and can visualize how small is the expenditure of resources per chip-set when compared to the value of the result to the community of designers. Thus, those designers who'd like to iterate their present designs, or take on a larger design, should take heart! There may be several MPC's in 1980! You instructors, coordinators, and designers can help to make sure this happens by letting other folks know what you've done, and how it was done. You can also help us

in this effort by submitting test results and short-form project reports for the MPC79 proceedings.

It is our sincere hope that MPC79 has provided a sufficient demonstration of the feasibility and practicality of remote-entry, fast-turnaround VLSI implementation, that it will lead to the funding and operation of a regular, scheduled VLSI implementation service for university students and researchers. We believe such a service will achieve an enormous return to the country on its investment, by greatly leveraging the human resources to be applied in the exploration of integrated system architecture and design.

ACKNOWLEDGEMENTS:

We wish to express our gratitude to all the folks who pulled together with us to make MPC79 happen, including our friends at Defense ARPA, at Micro Mask, and at Hewlett-Packard/ICPL.

We all owe a great deal to the dedication and efforts of the instructors and lab coordinators in the universities, who, working under great pressure and on a tight schedule, have done such a fantastic job with their design courses and project-labs this fall. We especially want to thank all the student designers for their enthusiastic response to the courses, and for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well!

Organizing and carrying out the implementation of these many imaginative VLSI design projects has been a very exciting and rewarding experience for us here at Xerox PARC/SSL.

The MPC79 Organizers

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5 January 1980