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To: MPC79.distribution

From: The MPC79 Organizers

Subject: **MPC79 Informational Message #5**

Filed on [MAXC]<Conway>MPC79.memo5

This is MPC79 informational message #5, the final general informational message prior to the design cutoff date. This message (1) discusses some issues related to the open "publication" in MPC79 of design layouts, (2) suggests some basic documentation that designers might include as comments within their CIF code, (3) presents some information concerning the starting frame and packaging, and (4) outlines future messages to be sent and a report to be produced concerning MPC79. Project lab coordinators should pass copies of this message on to the participating designers.

## 1. THE PUBLICATION OF DESIGN LAYOUTS: SOME ISSUES & OPPORTUNITIES:

The capability for teaching VLSI design courses in the universities and then providing students and university researchers with fast-turnaround implementation of design projects is quite new. Such new technological capabilities often raise novel and unpredicted legal and ethical issues. For example, a question that some designers out there may need to think about is what effect (if any) the open publication of the layout of their design may have on possible proprietary interests they or their organization may have in the design.

The implementation of the MPC79 multiproject chip set is being conducted by the implementing organizations on an open and public basis. There is really no alternative for us since we are using a prototype implementation system, and such things as data security (and also accounting, automated scheduling and planning, etc.) are being deferred to future efforts. The "printing" of the wafers containing the MPC79 projects will be much like the open "publication" of a group of technical articles. We ourselves aren't making any particular efforts to legally register or protect any of the information submitted for inclusion. Our major interest in this effort is to further test the feasibility of large-scale, remote-entry, fast-turnaround implementation of VLSI designs.

There are a number of traditional legal mechanisms for protecting novel designs or works of art (e.g. patents, copyrights, trade-secrets). The inclusion of a design in MPC79 doesn't necessarily preclude use of any of these traditional protections. These can be explored by individual designers (and/or their organizations) on a case-by case basis, as needed. However, do note that the inclusion of a project in MPC79 will result in a release into the public domain of a portion of the information associated with that design, and amounts to a limited form of "publication".

The novelty of this implementation effort will probably generate considerable interest. The various artifacts (plots, chips, chip photographs) associated with MPC79 will get a lot of public exposure. Various portions of these will be reproduced in technical reports and journal papers to be authored by some of the participants (both designers and implementers). It is even reasonable to expect that people at the various schools will examine and analyze available information about designs from other schools, in order to assess the differences in results at the different schools. The design files themselves will exist in several computers including those at the originating university. Thus it is

even possible that some design files could be be released into the public domain, as a function of the data security and the policies at the various intermediate sites they pass through.

O.K., that all sounds like some folks might lose a fraction of their potential proprietary interests in their designs if they include them in MPC79. However, there is another way to look at all this. Because of the large audience that will observe the results of MPC79, any marks placed into the layout itself which identify the design and designer will insure that a large peer group knows who did what. Thus, to whatever extent desired, a designer can obtain recognition in the usual form by obtaining "first publication" via this new medium of "publication".

And so, I suggest that designers at least put their name and/or logo, and perhaps a descriptive design title, right in the layout. If fairly large features on the metal level are used for this purpose, the information will show up well in chip photographs. If this is done, then future plagiarism can at least be recognized. Also, someone wanting to use a design would be able to identify, and then contact and negotiate with the original designer.

There are undoubtedly many interesting underlying issues lurking here that members of the technical community might discuss further with colleagues in law schools, business schools, and public policy groups. Perhaps a fundamental question is what legal and cultural traditions would best strike a balance between providing rewards and protection to the creative designer while at the same time stimulating research and innovation through the free exchange of ideas.

## 2. DOCUMENTATION OF DESIGNS: SOME SUGGESTIONS:

Because of the wide exposure of MPC79 artifacts, there will likely be requests for further information about particular designs or designers. For example, a company may wish to know how to contact the person who designed project X, in order to inquire about their availability for employment or consulting. We plan to list a moderate amount of basic information (such as designer names, schools, organizations, and project titles, as available) in our future technical reports on MPC79.

Those designers who are interested in receiving this sort of exposure should send some basic documentation along with their design files. A good way for designers to send this information is to insert it as CIF comments right at the beginning of their design files. I suggest that designer(s) include their name(s), school and department address, company name and address if they also work in industry, a short abstract describing their design, and pointers to any available or planned documentation or reports concerning the project.

## 3. STARTING FRAME AND PACKAGING INFORMATION:

The layout of the starting frame for MPC79 has been completed. There will be only one die size: 7696 X 6477 microns (~ 303 X 255 mils). This is the size as measured from scribe line center to scribe line center, prior to sawing up the wafers. The largest metal-line bounding-box that can be contained within the starting frame is 7548 X 5960 microns. The individual die sizes after sawing will be ~303 X 255 mils plus or minus a couple of mils, depending on how each die fractures below the saw cuts around its periphery (sorry about the English units, but the packaging industry still lives in the past and specs everything in mils). We recommend using standard 40 pins packages with cavity sizes of no smaller than 310 by 310 mils. (Use of larger cavity sizes, for example 340 X 340 mils, might be better since wire-bonding the pads near the edges of the chips would be made easier).

We have access to limited packaging capabilities, and a modest supply of 310 X 310 mil cavity 40

pin packages. We'll likely be able to do the packaging and wire-bonding for a few of the smaller isolated design groups that don't have any access to packaging equipment. We'd appreciate hearing from all the project lab coordinators so that we can learn of your school's capabilities and plans (or lack thereof) for doing the packaging of your MPC79 project chips. If you are planning to do your own packaging, you should either have packages in stock or be able to scrounge them from some local company, or else you should order them instantly in order to have them on hand in time when the wafers are ready. If you have access to local industrial help for packaging, and are able to arrange for some of the other schools to have chips packaged, let us know. Especially let us know if you plan to count on us to do your packaging.

The starting frame surrounding every die type will contain several test patterns having pads that can be be probed or wire-bonded that can be used to confirm that the process worked successfully and also to measure performance and certain electrical parameters. Included are four discrete devices (all having channels 5 microns long and 10 microns wide): (i) an enhancement mode FET, (ii) a depletion mode FET, (iii) a metal-gate field-oxide FET, and (iv) a poly-gate field-oxide FET. A ring-oscillator is included that can be used to measure the transit-time of minimum-sized devices. Also included are two Van der Pauw 4-point resistance measuring structures, to enable measurement of the resistances of specific poly and diffusion paths.

## 4. FUTURE MESSAGES & REPORTS ON MPC79:

Various announcement messages and messages to specific coordinators or designers will be sent out as needed between now and 4 December. Project lab coordinators should watch their mailboxes closely, especially during the final days before the design cutoff. Note: If project coordinators are ever unable to contact MAXC over the net, don't panic, but try again an hour or so later. In the unlikely event that MAXC goes down for more than on hour (especially if some time during the crunch of the last few days before the design cutoff), we will send out advisory messages to all coordinators via other HOST machines on the ARPANET.

After 4 December we will periodically send out status messages to help you track the progress of the maskmaking and wafer fabrication and to help you plan for the arrival of your wafers/chips.

During January and early February we will be seeking information from those participants who have by then tested their projects. We will be accumulating information about the results of the projects at the various schools, and will send out messages sometime in February summarizing this information.

During January and early February we will be documenting the results of MPC79 for inclusion as part of a Xerox PARC/SSL Technical Report by L.Conway, A.Bell, and M.Newell entitled something like "The Implementation of VLSI Systems". This report will likely be available by April '80. (If you'd like to receive a copy of this report, send a msg to Doughty@PARC-MAXC).

Well folks, were now entering the final week before the design cutoff. Good luck on finishing your projects! Watch your electronic mail to find how it all finally turns out.

Lynn Conway
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26 November 1979
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