MPC79 HP Letters:

HEWLETT hp PACKARD

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FROM: Mike Beaver

DATE: December 31, 1979

TO: MPC 79 Distribution

SUBJECT: MPC 79 Wafer Data

The attached data on the initial two runs for MPC79 represents in-process data from test wafers generated in the normal course of wafer fabrication plus electrical measurements taken on one of the wafers from each lot. This data is enclosed to give you some benchmark data against which you can compare your actual test results. Most of the electrical data was taken with a curve tracer and is subject to appropriate tolerances.

Additionally, wafer to wafer variations exist. If you need more precise data, you can generate it by probing the test devices on the border of each chip.

The follow-on run, from which you may receive additional chips will be similarly characterized. If you have specific questions about the processing, I will attempt to answer them.

Mike

Hewlett-Packard's Participation in MPC-79

The wafer fabrication segment of MPC-79 was performed by the Integrated Circuit Processing Laboratory of Hewlett Packard Co. which fabricated the MPC-78 project last year. This lab, directed by P. L. Castro, gives HP Labs the capability to do silicon wafer processing utilizing a wide range of modern processes and processing techniques. The NMOS process selected for MPC-79 utilizes more routine and standardized techniques and is optimized for ease of manufacture rather than density. This gave the highest probability of providing working circuits to the MPC-79 participants within the 2-3 week turnaround time that is basic to the MPC concept. In order to insure proper scaling of device dimensions as they were translated from design as-drawn dimensions to mask dimensions and finally to as-processed dimensions, HP-ICPL provided the needed information on the dimensional shifts that occur in the photomasking and etching operations. This information, together with the agreed upon valve of λ (2.5 microns) was used to properly alter the pattern data sent to the maskmaker. The resulting mask sets were used to produce two runs each of the two different mask sets, all of which were within the expected range for DC parameters and all of which provided working chips.

An annotated listing of the process follows. Certain minor steps, such as cleaning have been omitted from the listing for compactness.

Operation	Comment
Stress-Relief Oxidation	Thin oxide to separate the nitride fron the silicon
Nitride Deposition	Silicon Nitride layer deposited by Low Pressure Chemical Vapor Deposition
Diffusion Mask	This step defines and etches the nitride layer. The resulting nitride pattern defines the active (diffusion) areas.
Field Oxidation	Only the field is oxidized, isolating the active areas from each other. Again the nitride acts as a mask.
Field Implant	This implant is blocked from the active areas by the nitride. This implant raises the threshold of parasitic (field) transistors.
Nitride Strip	The masking nitride is removed
Gate Oxidation	A very clean gate oxide is grown

Enhancement Implant	Sets threshold for enhancement mode devices
Depletion Implant Mask	Defines which transistors will be depletion mode (load) devices. The photoresist itself is used to block the implant from the remainder of the wafer
Depletion Implant	Sets depletion mode device threshold
Poly Deposition	Poly silicon is deposited by Low Pressure Chemical Vapor Deposition
Poly Oxidation	The surface of the poly is oxidized
Poly Mask	Defines the poly areas
Source/Drain Predep	Provides doping for the transistor sources and drains. The poly protects the gate regions from being doped
N Oxidation	Drive-in and oxidation for source/ drain areas
Oxide Deposition	Low Pressure Chemical Vapor Deposition oxide deposited to provide additional insulation between poly and metal lines
Contact Mask	Opens contacts to diffusion and poly levels
Al-Si Evaporation	Metal fil deposition
Metal Mask	Defines and etches metal layer
Alloy	Alloy contacts to poly and diffusion levels to provide low resistance conduction paths
Plasma Nitride	Plasma deposited nitride layer for passivation (optional)
Pad Mask	Opens holes to bonding pads through plasma nitride

In addition to the actual wafer fabrication, electrical testing of the test pattern devices was performed to verify process parameters. Scribing and a limited amount of packaging of chips was also done at Hewlett Packard. The measured parameters are listed on the next page.

Run #	KDEI1	KDEI2	KDEI3	KDEI4
Mask Series	A	B	A	B
Thresholds (v) (recalculated)				
Enhancement	1.0	1.0	1.1	1.2
Depletion	4.6	3.9	3.9	3.8
Poly Field	21	20	16	21
Metal Field	21	20	14	20
Resistances (kΩ)				
Poly Resistor	6.4	8.4	6.7	7.0
Diffusion Resistor	3.6	3.9	3.2	3.6
Poly-Metal Contacts	2.3	2.6	2.1	2.15
Diff-Metal Contacts	1.4	1.4	1.0	1.1
Butting Contacts	3.6	4.3	3.15	3.2
Diffusion-Substrate Breakdown (v)	35.0	34.5	34.0	34.0
Osc Frequency @ 5 v	17.0	17.7	14.6	14.8
Process Parameters				
Gate Oxide Thickness Å	990	1000	1030	1040
Field Oxide Thickness Å	14600	14600	15400	14850
Poly Thickness Å	5370	5300	5040	4910
Intermediate Oxide Thickness Å	5000	5400	5100	5100
Diffusion Sheet Resistance Ω/□	17.2-17.8	16.2-17.1	16.3-17.0	16.4-17.3

The value of λ chosen for MPC-79 (2.5μ) was the result of a compromise between ease of processing, particularly masking operations, and density. A smaller value of λ could have been chosen but this was not considered to be a good balance of benefit and risk. The possibility of reducing λ for 1980 projects is being considered. Continued progress in reproducable etching techniques at Hewlett Packard (and the rest of the industry) should help to keep the risk low and processing time at a minimum.

HP-ICPL is happy to have participated in this joint project designed to greatly reduce the cycle time, from circuit design through packaged parts, of complex integrated circuits. We plan to work with the MPC Team for 1980 while plans are made to establish an industrial capability for fast turn-around processing in future years.

XEROX
PALO ALTO RESEARCH CENTER
3333 Coyote Hill Road
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January 14, 1980

Merrill Brooksby
Hewlett-Packard
1501 Page Mill Road
Palo Alto, CA 94304

Dear Merrill:

The effort to implement the fall '79 integrated system design projects for the universities has worked out very well. A total of 82 projects from 124 designers are included in the multiproject chip set. Many major projects have already been tested and several important ones have proven to work correctly. I've enclosed a short document which will give you and your colleagues an overview of the effort, some information on the participants, and a feeling for how things turned out.

It is my hope that MPC79 will serve as a powerful demonstration of the feasibility and the capability of fast-turnaround VLSI implementation, and thus confirm your early vision of how valuable such a service would be to the community of designers.

All of us here at PARC who participated in this effort want to thank you for your very valuable assistance in setting up the collaborative arrangements between Xerox PARC/SSL and HP-ICPL. None of this would have happened without your help these past two years.

Sincerely,

Lynn Conway

Lynn Conway
Manager, LSI Systems Area