7. Further Plans and Request for Feedback

This section presents our plans for further documentation and publication concerning MPC79, and describes how designers can participate by providing us with feedback about their projects. We encourage designers to test their projects, and to report on the results. The designers of interesting projects are encouraged to seek further publication of their work. Also covered are our plans for further packaging and distribution of chips, and for distributing photographs of the chips.

Feedback about Testing

We are very interested in learning the results of the functional testing of projects. We will highlight and strongly feature in our upcoming publications the work of those designers who provide us with the results of the testing of their projects. A questionnaire and a postage-free business-reply envelope is being distributed with this document; these can be used for submitting early test results and for providing us with other important feedback. Any test results that we receive by 31 January 1980 are sure to be mentioned in our upcoming publications.

On Friday, 28 December, shortly after the type-B wafers came off the line at HP-ICPL, the first project was tested and proved to function completely correctly (this was Jim Clark's "Hourglass" project, described in the attached short-form project report). We now know that the fabrication process has been successful, and that there are no systematic errors in the overall MPC79 implementation effort. And so, the time has finally arrived to find out if *your* project works! We're looking forward to hearing from you and learning the results.

The MPC79 Proceedings

We are compiling a proceedings documenting the MPC79 effort, to be published as a Xerox PARC/SSL Report entitled: *Proceedings of the MPC79 Multi-University Multiproject Chip Set Project*, edited by A.Bell, L.Conway, R.Lyon, M.Newell. This proceedings will include (i) photos of all the different die types, (ii) information from the MPC79 ARPANET message traffic, (iii) material from this implementation documentation, (iv) information about the MPC Implementation System, and (v) feedback from the universities. *We especially hope to include a collection of short-form project reports describing a number of the MPC79 projects.*

The MPC79 Proceedings will be printed in large quantities and distributed widely in the universities and in industry. For any of you designers who'd like some visibility, now's your chance! Be aware that there is an intense and growing demand for systems folks who know all about VLSI architecture and design. This demand provides students just finishing degrees with many exciting employment opportunities in industry, provides great opportunities for those interested in teaching, and provides university faculty and research staff members with many opportunities for industrial consulting.

Designers who'd like to see their projects featured in the upcoming MPC79 Proceedings should do the following: (i) Fill out the attached questionnaire, indicating that you plan to submit a report. (ii) Return the questionnaire to us by 31 January 1980, so that we can plan to include your report. (iii) Prepare your report: This can be a short summary of your class project report. Try to provide a hierarchical view of your project, both in words and pictures, but in a compact amount of space. Include some information about yourself, and about the tools used to create your design. Two or three pages of text, followed by two or three pages of diagrams should be adequate for all but the largest projects. See the sample short-form project report appended to this section, to get an idea of what we're looking for. (iv) Send the report to us by 29 February 1980.

Other Places to Publish Your Work

Most of the designers participating in MPC79 are university students, working on projects as part of their VLSI design courses. It might not occur to these students that, by completing a novel VLSI design project, they may have done something worth reporting on. It appears to us that many of the projects have highly innovative architectures and novel design features, and that a few students have undoubtedly done important, original work (of course, there are also some highly visible exceptions!). Thus, it may prove easier than you think to have your work published. We suggest that all students who have successfully completed interesting projects seek publication of their work in appropriate journals, proceedings, or magazines. If you aren't sure how to go about this, talk it over with your instructor or faculty advisor.

Some good places to publish are as follows: Major projects having innovative architectures, especially those that tested successfully, should seek publication as soon as possible as reviewed papers in the appropriate IEEE or ACM technical journals. An alternative to this would be to submit papers to any of the upcoming VLSI design conferences to be held at the major universities. Many projects involved the use of novel design aids; papers on these could be submitted to the annual IEEE/ACM Design Automation Conference. Many of the projects could lead to excellent articles in Electronics, Computer Design, Electronic Design, and any of the personal/hobby computer magazines such as Byte. You may also be interested to learn that Doug Fairbairn has started the new magazine LAMBDA, about VLSI design, for the VLSI system designer. He is quite interested in featuring novel MPC79 projects in upcoming issues of LAMBDA. To contact him write to: LAMBDA Magazine, P.O.Box 50503, Palo Alto, CA 94303.

Plans for Packaging More Chips

Since we have only limited packaging capabilities, we are distributing only one packaged chip per project for most of the projects in the shipments going out on 2 January 1980. In some cases, where we know that projects will undergo immediate functional testing, we are distributing two or three packaged chips per project.

There will be a need for further packaging. Probably the largest demand for this additional packaging will be for projects having multiple designers, so each designer can have a copy. We are shipping a moderate number of unpackaged chips to each coordinator in the shipment of 2 January, and coordinators may be able to make local arrangements for the packaging of these additional

chips. We may do some additional packaging here at PARC, and we may also be able to arrange for further packaging to be done elsewhere.

So, if you'd like to get hold of more packaged chips, talk to your lab coordinators. They may be able to make the local arrangements, or they may relay your request on to us. We'll expedite the packaging of additional chips for those who plan to do some serious functional testing, especially for the larger projects (if your project has a very large area, you may need to test several copies of it, in order to separate possible design errors from possible fabrication defects).

Plans for Making Chip Photographs

In the near future, a commercial photographer will be producing 8" x 10" photographs, both in color and in B/W, of each of the MPC79 die-types. We'll distribute copies of these photographs to each university, along with information on how to order more copies from the photographer.

We may arrange to leave a set of wafers and wafer-maps with the photographer, and try to set up arrangements so that participants can have photographs taken of their *individual* projects, ordering them by ProjectID. Many folks will want to obtain photographs of their individual projects to use with papers they are publishing, to have as souvenirs, or to use as frontispieces for their resumes! Also, some schools may want to compile sets of photos of their successful projects. If we're successful in making the arrangements for ordering individual project photos, we will announce them at the time we return the first set of 8" x 10" overall chip photographs.

Our Plans for Reports on VLSI Implementation and on the MPC Implementation System

During the Spring of 1980, we'll be writing several Xerox PARC/SSL Reports concerning VLSI implementation that may be of interest to those who wonder about what went on "behind the scenes" to pull off the implementation of MPC79. The overall subject of VLSI implementation will be discussed in *The Implementation of VLSI Systems*, by L.Conway, A.Bell, and M.Newell. A detailed description of the internal structure and operational use of the MPC implementation system software will be given in *The MPC Implementation System*, by A.Bell and M.Newell. As soon as these reports are printed, we'll send some copies out to the EE/CS departments at the participating universities.

Conclusion

Good luck on your functional testing. Be sure to send in those test results and project reports! MPC79 has been very exciting and a lot of fun for us. We hope the same is true for you!

Happy New Year!

Lynn Conway, Alan Bell, Martin Newell, Richard Lyon, Richard Pasco
1 January 1980

An nMOS System Clock

by
James H. Clark
Computer Systems Laboratory
Stanford University

Introduction.

This is one of two projects by the author that are included in MPC79. These two projects comprise the principal parts of a Geometry Engine for doing floating-point operations on 4-component vectors. The final chip will consist of one copy of the "Hourglass" project described here (BK-5, Clark2SU) and four function units, each one of which is two copies of the "Geometry Engine" project in MPC79 (BK-8, ClarkSU), with appropriate numbers of the principal bit-slice.

Each of the function units of the final chip has three registers, an ALU and a stack. The units can be microprogrammed for a variety of different functions. Specific microprograms currently being implemented perform four of the computation-intensive tasks common to much of computer graphics: 4x4 matrix transformations; clipping and scaling of polygons, lines and characters; and 4x4 determinants. In one parallel/pipeline organization, a set of 12 identical chips transforms four-component vectors, clips to six planes, and scales three coordinates to the system of the destination display at the rate of about 3500 lines (or 900 four-sided polygons) every 1/30 second, assuming $\tau = .2$ nsec. Some interesting characteristics of the final system are: 1.) a large number of functions are accomplished with a very simple, homogeneous organization, 2.) each chip is locally a synchronous system that communicates asynchronously with other chips, as described in detail below, and 3.) using 1 micron line widths, it will be possible to fabricate the 12-chip system on a single chip, with a factor of 4 performance improvement over the figures given above.

Because the organization described above requires that each chip communicate reliably with other chips, the author chose a self-timed, 4-cycle communication protocol that avoids synchronization failure, as described in Mead & Conway by Chuck Seitz. The clock circuit "Chuck's Hourglass" described here is an adaptation of the pipeline clock given by Seitz that generates two-phase, non-overlapping clock signals.

Description.

The main circuit for the clock is shown in Figure 3. The oval shapes shown in this diagram are asymmetric delay lines. These delay lines propagate high-going levels with a delay governed by the inverter pair delay (plus capacitive loading); low-going levels propagate very quickly [cf. Ch. 7, Mead & Conway]. The plan view of the layout for the chip is shown in Figure 1.

This clock has a very long Phi1 and a relatively short Phi2. By convention, throughout the Geometry Engine, all registers are loaded and ALU's are precharged on Phi2, and computation and bus precharging take place on Phi1. Registers are also refreshed on Phi1. This convention can be likened to a standard TTL clock in which the TTL clock pulses occur on Phi2.

To understand the behavior of the clock, refer to Figure 3 and assume that the clock RUN level has been low sufficiently long for the bottom input to the 3-input NOR gate (call it gate 3n) to be at logic level 0. In this state, the output of 3n will be 0, PAUSE is 1, Phi1 is 1 and Phi2 is 0. A short delay after RUN is asserted, the output of this NOR will be a high-going signal presented to the input of delay line d2, and Phi1 will go low. After the delay of d2, a high is presented to both inputs of the Phi2 gate, causing Phi2 to go high. On leaving delay line p2, the inverter reverses the polarity of the transition, and a high level is very rapidly presented at the bottom input of gate 3n, causing its output to go low, thereby lowering Phi2. On the second time around the loop, the transition is low-going and hence fast through d2 and p2, and delay lines d1 and p1 determine the time required for the signal to propagate. If LongTick is asserted before p1a goes high on the second time around, Phi1 is lengthened by the delay difference between taps p1a and p1b.

This clock differs from that given by Seitz in several ways. First, Phi1 and Phi2 are obtained directly from the delay line; hence it is very easy to select the amount of non-overlap between Phi1 and Phi2. A second difference is the Pause signal. This signal is asserted when the clock has completed a cycle, i.e. the end of Phi1, but is not running. Its use is peculiar to this particular application.

To avoid synchronization failure, the clock incorporates two sets of 4-cycle communication circuits. One set is for normal pipeline communication, similar to that given by Seitz, and the other set is peculiar to the particular way that this clock is used in the present context. Figure 2 illustrates the circuits that handle the 4-cycle handshaking, and their effect on the RUN signal is shown in Figure 4. Incoming requests(ReqIn) start the clock if it is stopped waiting for an input request(LoadInput is asserted). Likewise, the clock stops if the control asserts LoadOutput and the previous output request has not been acknowledged. The behavior of these two blocks is precisely that given by Seitz, but the circuit implemented here avoids his circuit in which "ground" is supplied to an inverter by the output of another inverter, thereby avoiding unusual pull-up/pull-down ratios.

One feature not shown directly but implied by the pad labeled "Fast" in Figure 1 is a level of multiplexing that selects between two global clock periods. By not asserting Fast, everything is lengthened. The intent here was to provide a way that the clock could be slowed down by 30% over the normal speed to allow testing the circuit being driven by it without concern for speed problems.

Test Results.

The clock chip was bonded and tested on 12/28/79. All worked as planned except that the period was approximately a factor of two longer than expected. This is presumably due to having neglected effects of stray capacitances in the delay lines. It is easily compensated for by eliminating some of the capacitive loading in the delay-line cell. The measured periods in nanoseconds were:

LongTick	Fast	d2	Phi2	d1	Phi1
0	1	60	137	50	430
0	0	60	150	50	560
1	1	60	137	50	590
1	0	60	150	50	840

For the purposes of the test chip, one set of ReqAck blocks was disconnected. The other set of blocks were connected as follows: the ReqOut of one block was connected to the ReqIn and LoadIn of another; likewise, the AckOut was connected to AckIn. LoadOut was set to be the complement of the ReqOut. This connection caused a ReqOut to be generated every other cycle of the clock; the corresponding AckIn was generated on the alternate cycles. In this way the clock sent and acknowledged its own requests.

The project layouts were done using the ICARUS interactive circuit layout program. The total design and layout time for the clock was approximately two weeks. The Geometry Engine design time was three months, and layout time was approximately three weeks. A very crude design rule checker was used to check parts of the circuit. Helpful assistance was given by Dick Lyon and Martin Newell, of the LSI Systems group, Xerox PARC/SSL.

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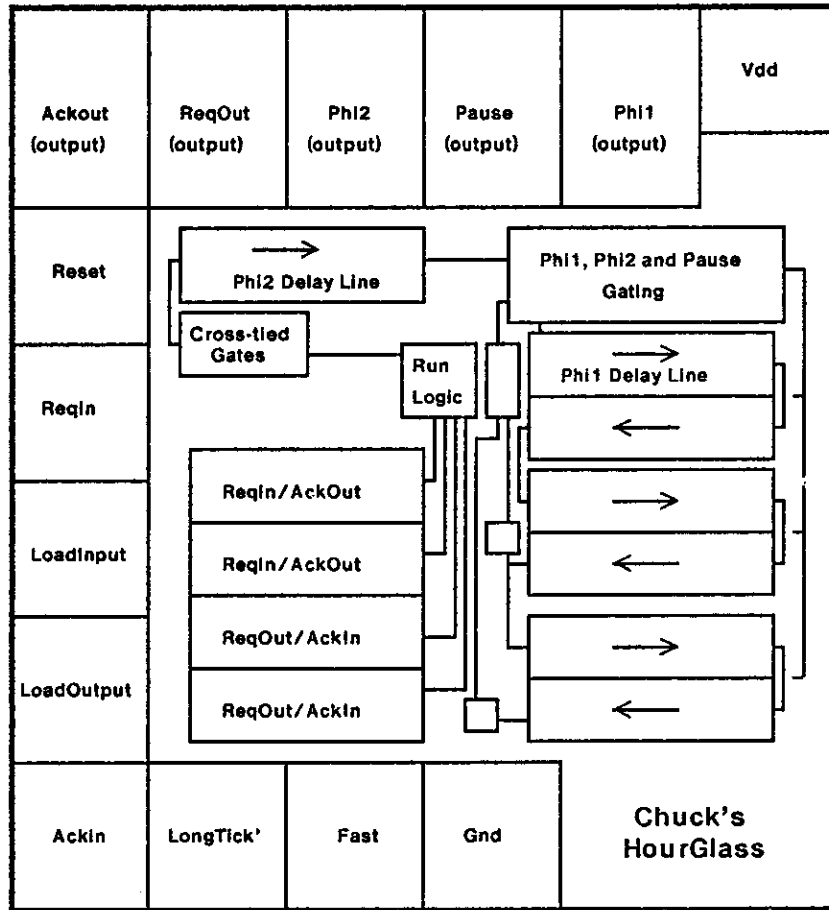*Telephone:* (415) 497-1414
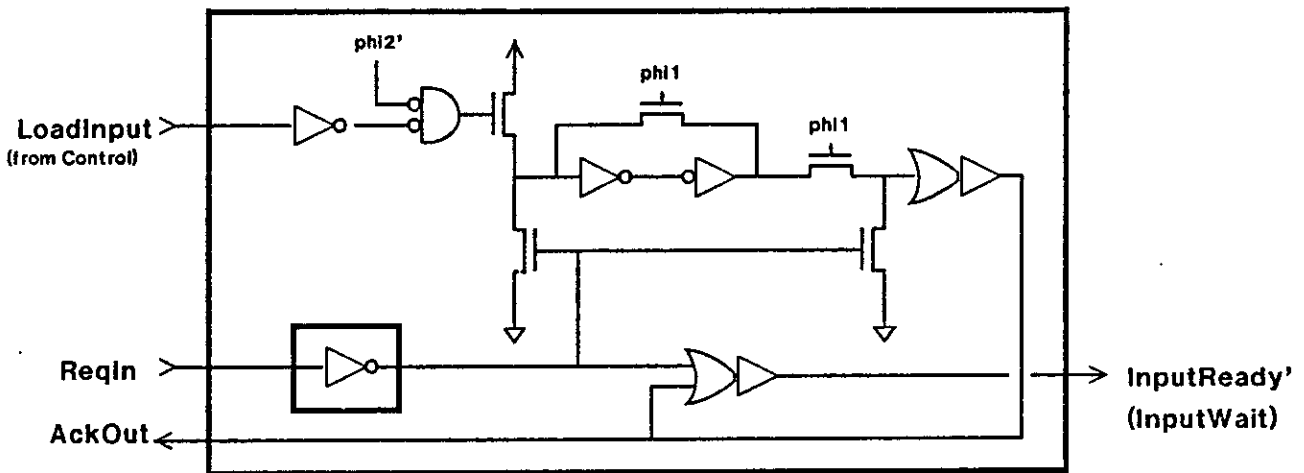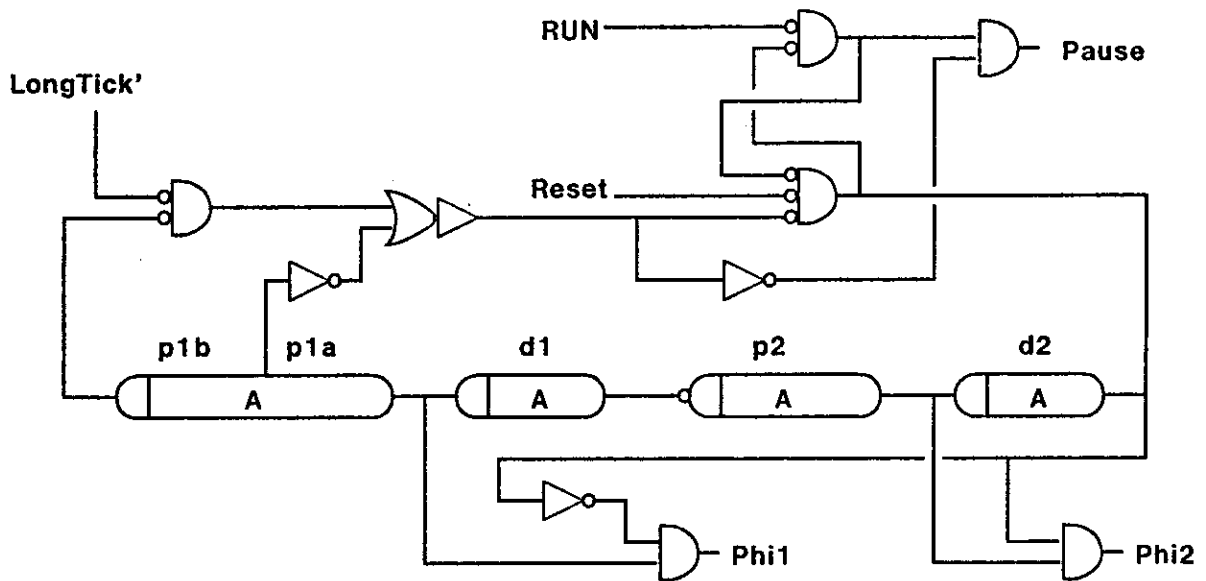
Figure 1. Clock Chip Floorplan, MPC79-BK.

Figure 2. ReqIn/AckOut Block. The Circuit for ReqOut/AckIn is identical
except that the indicated inverter is replaced with wire and inter-
change "out" and "in".

RUN = 0 before end of Phi1 stops clock synchronously
    with Phi1 high.
RUN = high-going starts clock with Phi1 going immediately low.

d2 = delay from low-going Phi1 to high-going Phi2.
p2 = approximate Phi2 high time.
d1 = delay from low-going Phi2 to high-going Phi1.
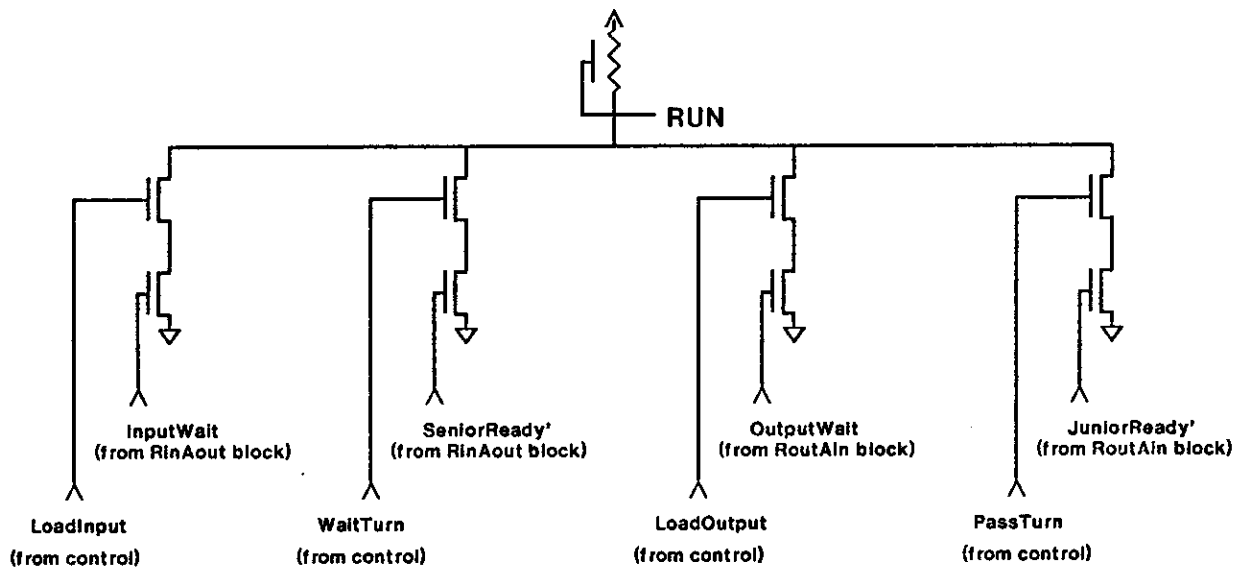p1 = Phi1 high time.

Figure 3. Clock Circuit.

Figure 4. Run Logic.

A Questionnaire for the MPC79 Designers

It would be extremely helpful to the evaluation of the MPC79 prototype implementation system if each participant would take the time to fill in the following questionnaire. We would appreciate both positive and negative feedback - we would like to know what you liked about the service, so that we can be sure to retain those aspects in future implementations, as well as what you did not like together with suggestions for improvements, so that we can try to do better next time.

Please feel free to fill in as much or as little as you desire - all sections, including your name, are optional. If you want to express an opinion about only one topic then fill in just that topic. On the other hand, add additional sheets if you need more space than that provided.

Please mail the questionnaire back to Ms. Lynn Conway, Xerox PARC, 3333 Coyote Hill Road, Palo Alto, CA 94304. Addressed, postage-paid envelopes have been included for your convenience. The target date for getting the questionnaires back is January 31, 1980. This is intended to give sufficient time for most people to test their projects.

Your Name: **Project ID:**

University/Department: **Industrial Affiliation (if any):**

Degree sought (if any):   **Expected graduation date:**

Have you tested your project?:   Yes ☐; No ☐.
    If so, did it work?:   Fully ☐; Partially ☐; Not at all ☐.
    If not, by when do you expect to test it?:
    Further testing information:

Will you be submitting a short report of your project,
    by February 29, 1980, for inclusion in the MPC79 Proceedings?   Yes ☐; No ☐.

Are you planning to report on your project elsewhere?:   Yes ☐; No ☐.
    If so, in which journal, magazine, or proceedings?:

Did you receive copies of the MPC79 Informational Messages?:   Yes ☐; No ☐.
    If so, what did you think of their:
    Content: Too much ☐; OK ☐; Too little ☐.   Clarity: Good ☐; OK ☐; Poor ☐.
    Comments:

Implementation Documentation (i.e. that sent along with the chips)
    Clarity/conciseness: Good ☐; OK ☐; Poor ☐.   Sufficiency: Good ☐; OK ☐; Poor ☐.
    Is the information about your project correct in the documentation?:   Yes ☐; No ☐.
    Comments:

What did you like most about the MPC79 implementation service?:

What did you dislike most about the service? What did you think of working to deadlines?:

Did you find the cell library useful? How could it be improved?:

Any ideas about how to improve the service, to better support the VLSI design courses?:

Other comments (feel free to be verbose, use extra sheets as necessary):

Your Address(es)/ Phone #(s):