4. Starting Frame Documentation

The following pages describe the structure, function, and use of the various objects in the MPC79 starting frame (a starting frame is the set of all those layout artifacts, not associated with any particular design project, which serve to convey a project chip through maskmaking, wafer fabrication, and electrical testing). Included are the die dimensions and layout, the scribe-line profile, and descriptions of the alignment marks, layer codes, critical dimension testers, etch test patterns, die identification codes, discrete test transistors, ring oscillator, test resistors, contact tester, layer tester, and die code-letters.

Inter-Office Memorandum

To	MPC79 Distribution	Date	December 17, 1979
From	Rich Pasco	Location	Palo Alto
Subject	MPC79 Starting Frame	Organization	PARC-SSL-LSI

XEROX

Filed on: [ivy]<Pasco>MPC79>StartingFrameMemo.Press

This memo describes the Starting Frame used in generation of the MPC79 chip set. The Starting Frame is a collection of items common to all chips in the set. It consists of a scribe line to make it easier to cut the wafer into dice, and a top strip containing alignment marks, lithography test patterns, and test devices.

Die Dimensions and Layout

Overall Die Dimensions: 7696 x 6477 microns

The dimensions are:

Vertical:

Scribe-Line Profile:	66 microns.
Setback:	21 microns.
Top-Strip:	370 microns.
Setback:	20 microns.
Maximum project:	5926 microns.
Setback:	8 microns.
Scribe-Line Profile:	66 microns.
Total:	6477 Microns (=255 Mils)

Horizontal:

Scribe-Line Profile:	66 microns.
Setback:	8 microns.
Maximum project:	7548 microns.
Setback:	8 microns.
Scribe-Line Profile:	66 microns.
Total:	7696 Microns (~303 Mils)

Scribe-Line Profile.

The scribe-line profile includes the scribe line itself and a metal band. The scribe line itself is a coincident contact cut, diffusion, and overglass cut, 41 microns to either side of center. This removes all oxide, allowing the wafer saw to cut directly into the silicon wafer. 10 microns from the scribe line is a 15-micron-wide band of metal which serves as a visual guide to the saw operator and separates the project area from the saw area.

Alignment Marks.

Two kinds of alignment marks are provided. In the upper left corner of the die is a square appearing on all layers; this provides a gross alignment indicator. For fine alignment, to its right are a sequence of "Squares" and "Fortresses" as described in Section 6.1 of the Xerox PARC/SSL Report, *A Guide to LSI Implementation*, 2nd Edition, by Hon & Sequin (Sect. 7.1 in 1st Edition).

Layer Codes, Critical Dimension Testers, and Etch Test Patterns (Ells)

Below the alignment marks appears a set of six similar patterns, one for each of the six layers. Each consists of three items: the layer code, from {DIF, IMP, POL, CUT, MET, PAD}, a cross-shaped critical dimension tester, and a set of Ell-shaped etch test patterns.

Critical Dimension Testers are crosses with line widths as follows:

DIF	5.0 micron	CUT	5.0 micron
IMP	10.0 micron	MET	10.0 micron
POL	5.0 micron	PAD	10.0 micron

Etch test patterns (ells) are 65 microns high. Smaller ells, with 2.5 micron linewidth and spacing, are nested inside the upper right corner of larger ells with 5 micron linewidth and spacing. In addition, there is a vertical 5-micron-wide bar down the left side of the pattern to make measurement easier.

The polysilicon critical dimension tester and etch test pattern are repeated over thin oxide (diffusion mask) to the right of the alignment marks.

Although digital stretching of diffusion layer is specified for all active devices on MPC79, no stretching is performed on critical dimension testers and etch test patterns.

Identification Code

Each die has a unique seven-character identifier, e.g. "MPC79AF". The first five characters "MPC79" indicate that this chip is a 1979 MultiUniversity Project Chip. The next two characters indicate the wafer and die, respectively. There are fourteen die types (B through O) in MPC79 on two wafers (A and B); thus code letters are in {AB, AC, AD, AE, AF, AG, AH, BI, BJ, BK, BL, BM, BN, BO}. For example, letters "MPC79AB" indicate that this is die type B on wafer type A.

Discrete Test Transistors

Discrete devices are shown for measurement of dc parameters such as threshold voltages. Figure 1 shows the location within the starting frame and pad connections for the test devices.

Four devices, with sources and gates are bussed together, but having separate drains, are provided. All have 4 lambda (10 microns) wide by 2 lambda (5 microns) long channels. There is one device of each of the following types:

Metal gate, field oxide.
Poly gate, field oxide.
Poly gate, thin oxide.
Poly gate, thin oxide, Ion Implant (depletion mode),

Ring Oscillator

The ring oscillator is used to estimate the speed of devices made using this process. It consists of nineteen identical inverters in a circle, and a twentieth as a buffer to drive a line to a standard output pad, where there is more buffering to drive the outside world. Each inverter in the circle is minimum geometry, K=4. Pulldowns have 4 lambda (lambda = 2.5 microns) wide by 2 lambda long channels. Pullups have 2 lambda wide by 4 lambda long channels. Since the oscillator period T equals the delay twice around the loop, the inverter pair delay is T/n, where n is between 19 and 20 since eighteen of the inverters drive only one similar inverter but the nineteenth drives two.

Test Resistors

There are two Van Der Pauw structures, one in polysilicon and one in diffusion, with identical geometry as shown in Figure 2. In a Van Der Pauw structure, there are two pads at each end of each resistor to allow separate current feed and voltage sense paths to the layer being tested, so that probe and contact resistance does not introduce error into the measurement. These devices provide a long aspect ratio (266.5 to 280.5 squares, depending on how corners are treated*) path of minimum width (5 microns = 2 lambda). Because of edge effects, sheet resistivity estimates from these measurements (sheet resistivity = total resistance divided by aspect ratio) are only approximate for other than 2 lambda wide lines.

*For further information on paths that go around corners in sheets of resistive material, see D. Vitkovitch, Ed., *Field Analysis, Experimental and Computational Methods*, D. Van Nostrand Co., Ltd., 1966.

Contact Tester

The contact tester has 3 sections, each consisting of 100 Mead & Conway minimum geometry contacts in series: metal-diffusion, metal-poly, and diffusion-poly-butting, with pads at each end and between each section. There should be continuity between any pair of pads.

Layer Tester

This layer tester was designed by Rick Davies and described in Hon & Sequin, *A Guide to LSI Implementation*, Second Edition, Section 6.2.1 (was 7.2.1 in First Edition) A polysilicon snake zigzags across thin oxide (diffusion mask), forming a large transistor. (Channel 2095 lambda wide by 2 lambda long). On top of this, a metal snake zigzags between two interdigitated metal combs, crossing the poly snake many times.

There should be continuity between:

Metal Snake In and Metal Snake Out
Poly Snake In and Poly Snake Out
Diffusion Left End and Diffusion Right End (when Poly Snake is high)

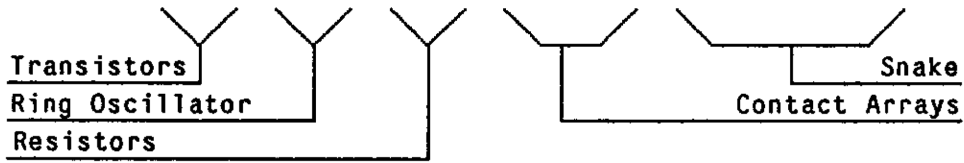
There should be no continuity between:

Metal Snake and Top Metal Comb
Metal Snake and Bottom Metal Comb
Poly Snake and Top Metal Comb
Poly Snake and Bottom Metal Comb
Poly Snake and Metal Snake
Poly Snake and Diffusion (be careful - thin gate oxide)
Diffusion and any Metal feature
Diffusion Left End and Diffusion Right End (when Poly Snake is low)

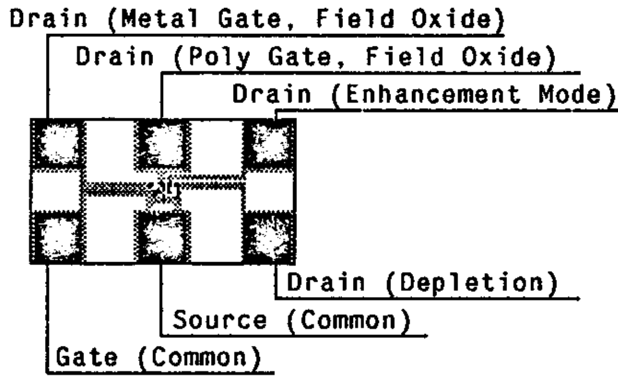
Die Code Letter

The die code letter is repeated in the upper right corner of the die. Hopefully this will be legible to the unaided eye.

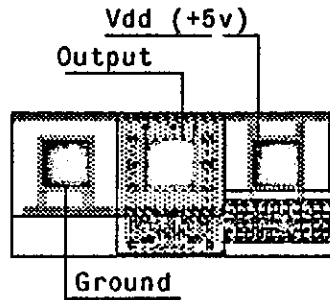
MPC79 Starting Frame Test Devices



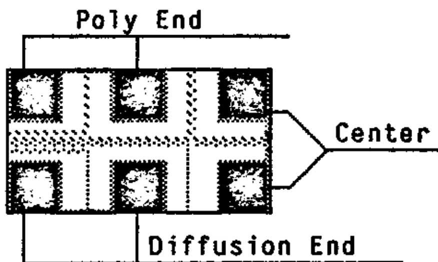
Transistors



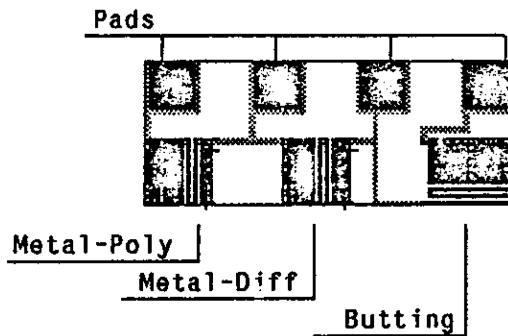
Ring Oscillator



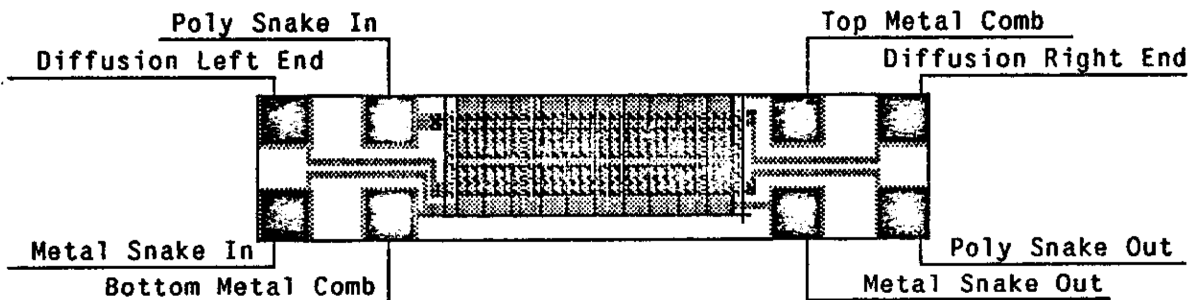
Resistors



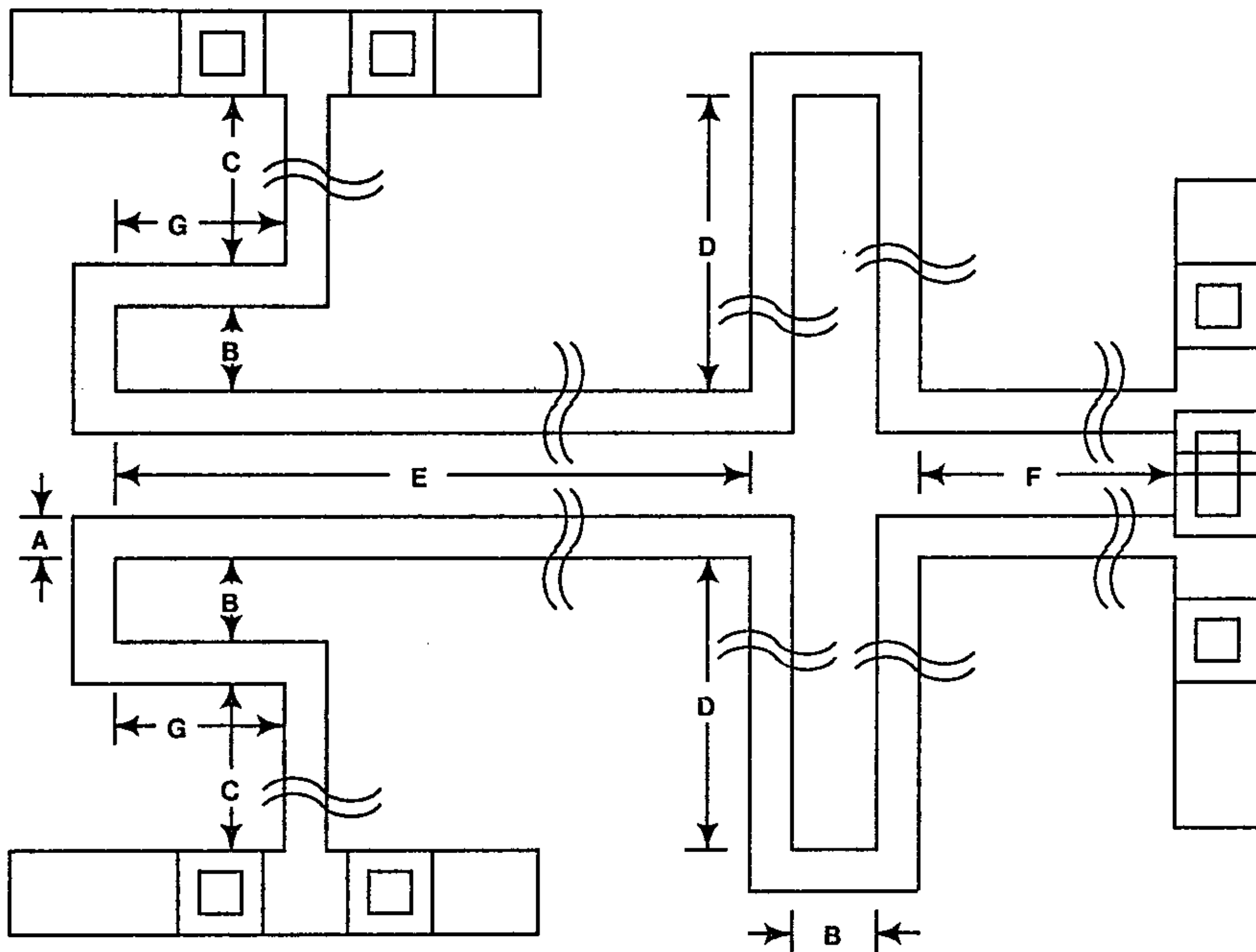
Contact Arrays



Snake



XEROX PARC	Project	Title	File	Designer	Rev	Date	Figure
	MPC79	Starting Frame Test Devices	TestDevices.Press	Pasco	A	12/11/79	1



Dimension	Lambda	Microns
A	2	5
B	4	10
C	60	150
D	68	170
E	180	450
F	72	180
G	77	192.5
Inside Path Length*	533	1332.5
Outside Path Length*	561	1402.5

*Inside Path Length is shortest path, following inside edges.
Outside Path Length is path following outside edges.

XEROX PARC	Project MPC79	Title Test Resistors	File Resistors.Sil	Designer Pasco	Rev A	Date 12/11/79	Figure 2