1. Introduction and Overview

This document provides a collection of information and instructions for use by the VLSI system designers participating in the MPC79 multi-university multiproject chip-set.

This introductory section provides background information about MPC79, about the context in which it occurred, and some reasons why the effort was undertaken. Summaries are provided of the participating universities, of the organizations involved in the implementation effort, and of the overall schedule of MPC79 events. This background material may help provide the general reader with a visualization of what MPC79 was all about.

Section 2 contains important basic information that the designers can use to identify their packaged project chip and to prepare the chips for testing. Section 3 contains project locator maps and a complete list of all projects and designers. Sections 4 and 5 provide information about the starting frame and electrical test results. Section 6 presents a complete set of unmarked wire-bonding maps. These maps can provide the designers and the general reader with a visualization of the scope of the MPC79 projects and the overall effort. Finally, Section 7 discusses our plans for packaging and distributing more chips, for taking and distributing chip photographs, and for writing additional reports concerning MPC79.

The Background and Context of MPC79

Since 1976, the LSI Systems Area of the Systems Science Laboratory (SSL) at Xerox Palo Alto Research Center (PARC) has conducted research in the architecture and design of integrated systems. One focus of that research has been the exploratory development, in collaboration with the Caltech Computer Science Department, of new design methodologies which simplify integrated system design so that this capability can be more quickly acquired and more widely practiced by system designers than was possible in the past.

Through this research, new design techniques have evolved and have then been debugged in actual practice in the university classroom, and during in-house short courses. This has been a process of discovery and iteration, moved forward by teaching design techniques to university EE/CS students and to practicing EE's and computer scientists, and then having the students undertake VLSI design projects as part of their course experience. Groups of these VLSI projects, and thus the design methodology itself, have been subjected to the "acid test" of actual implementation and testing.

Our teaching and implementation activities have thus been an integral part of our research methodology. There has been success in this effort, leading to the publication of the textbook "Introduction to VLSI Systems", by C. Mead and L. Conway, Addison-Wesley, 1980, describing the new design techniques. A number of major universities, including MIT, CMU, Stanford, Caltech, and U.C. Berkeley, now offer standard courses in VLSI system design based on this textbook.

By early 1979 it had become clear that a demand for fast-turnaround VLSI implementation would develop that was far beyond our ability to supply using our early ad-hoc methods. We then conceived the idea of developing what amounts to an "operating system" to interface a large number of remote users with centralized maskmaking, wafer fabrication, and packaging facilities, making automated responses to electronic messages from users, juggling the many constraints involved, and handling the vast logistics required to coordinate the overall implementation effort.

We were convinced that such a system could significantly reduce implementation turnaround-time, could reduce by about two orders of magnitude the cost per design-iteration compared to that normally incurred in the industry, and could bring access to the fabrication process to a much larger technical community than in the past. We conceived of evolving such a system using the same method used to develop the design methodology: By design, use, and iterative debugging in the universities, with the system used to provide an implementation service to university designers.

The architecture of a prototype implementation system was undertaken and completed during the summer of 1979 by Alan Bell and Martin Newell. They completed the design and coding of the system during the early fall of '79, in time for use to support the fall 1979 VLSI design courses.

The MPC79 effort was then mounted, for the purposes of (i) continuing our support of university VLSI design courses by providing the implementation of student-project designs, (ii) demonstrating the feasibility and general capabilities of such VLSI implementation systems to a wide technical community, and (iii) refining our ideas concerning the architecture, design, and operation of such systems, by running a major operational test of a prototype system.

It is unusual and perhaps somewhat controversial for us to mount such vast experiments in a large university community. There are great risks involved: risks of failure and the risks associated with presenting undebugged technology and techniques to a large group of students. However, we've found the universities eager to collaborate and to run these risks with us. It is exciting and we believe it is appropriate for university students to be at the forefront, sharing in the great adventure of developing and applying new knowledge.

The Participating Universities and Designers

The user community for this demonstration was composed primarily of EE/CS students taking the courses in VLSI system design at major universities throughout the United States, along with a number of university faculty and research staff members undertaking major VLSI system designs.

The MPC79 chip set contains a total of 82 VLSI system design projects from a total of 124 participating designers. Designs were included from VLSI design courses at M.I.T., Caltech, Stanford University, Univ. of Illinois, and Univ. of Rochester. MPC79 also includes a number of designs by faculty and research staff members at M.I.T., CMU, Stanford, U.C. Berkeley, Univ. of Washington, Yale University, Univ. of Bristol (England), and Univ. of Colorado (Colorado Springs).

The project-oriented university VLSI design courses were run on a very tight schedule: The courses began in mid-September. By early November, students had learned enough about the basics of VLSI design to originate a project concept and begin design work. The design cutoff date was 4 December 1979. Thus, students learned how to design in about 6-7 weeks, and then completed a project in the remaining 6-7 weeks of the course. Most large research designs in MPC79 took somewhat longer to create, and some of these are iterations of earlier designs by the researchers.

This has resulted in quite a wide range of interesting designs, as you can visualize by looking at the maps in Section 6. They range from small individual student projects, on through to large efforts by groups of designers. Some are very large, ambitious, team projects by university researchers, using sophisticated design aids of their own creation.

MPC79 was run on a schedule to deadlines, in order for fast-turnaround maskmaking and wafer fabrication to be scheduled. We did not censor designs: If a design met certain prearranged requirements for space allocation, consisted of syntactically correct code, and was submitted by the coordinators as "finished" before the deadline, then it was included. In a few cases, designers took on a bit too much for the available time (if you look closely at the Sect. 6 maps, you'll find cases where last-minute panic changes led to glorious disasters). But that was all part of the happening!

Organizations involved in the implementation effort

Several other organizations collaborated closely with us in conducting this demonstration: Data communications (electronic messages, design file transfers) were supported using the ARPANET; maskmaking was done by Micro Mask, Inc., using an electron-beam maskmaking system; and wafer fabrication was done by Hewlett-Packard's Integrated Circuit Processing Laboratory. Further information on this university-industry-goverment collaborative effort will be given in an MPC79 Proceedings and in several technical reports, to be published in the spring of 1980 (see Section 7.).

For an overview of the flow of information and artifacts through these various organizations, see the MPC79 Flowchart at the end of this section (that same flowchart, along with a page of text describing MPC79, is printed on the "document chips", one of the chip types in each wafer set!).

MPC79 implementation schedule

Following the design cutoff time of 5:00 pm, Tuesday December 4, we started final processing of the implementation requests. At 10:00 am the next morning we took the merged mask-specification data to Micro Mask. Delivery of the masks was pipelined with the early fabrication steps, with the first mask of both mask sets being delivered at 5:00 pm, Thursday Dec. 6. By then, HP-ICPL had already started the processing and were ready for the first masks. Processing continued normally except for one major contingency: the failure of a poly-deposition system (causing a delay of about 8 days for repairs, and leading to an additional delay in wafer processing due to the Christmas holidays). At 10:00 am on Dec. 28, the B wafers were ready, and on Monday Dec. 31 the A wafers were ready. Packaged chips, with custom wire-bonding maps, were shipped out to all participants on 2 January, 1980. Thus the implementation turnaround-time for MPC79 was 29 days.

Most of this document was itself produced automatically by the MPC implementation system, directly from the design-file data-base and archived records of the MPC79 die-layout-planning/design-merging process. This method of rapid document-creation enabled us to return this material in a timely way to the designers, right along with their packaged chips.

Looking Ahead

Many of the MPC79 designers are already looking ahead, making plans for iterating their present designs, and dreaming up even more ambitious design projects. Many other university students will want access to VLSI implementation, so that they too can have the experience of learning to design in a state-of-the-art technology by actually *doing it.* The demand for such services may build

rapidly, once folks know that it is feasible and can visualize how small is the expenditure of resources per chip-set when compared to the value of the result to the community of designers. Thus, those designers who'd like to iterate their present designs, or take on a larger design, should take heart! There may be several MPC's in 1980! You designers can help to make sure this happens by letting other folks know what you've done, and how it was done.

It is our sincere hope that MPC79 has provided a sufficient demonstration of the feasibility and practicality of remote-entry, fast-turnaround VLSI implementation, that it will lead to the funding and operation of a regular, scheduled VLSI implementation service for university students and researchers. We believe such a service will achieve an enormous return to the country on its investment, by greatly leveraging the human resources to be applied in the exploration of integrated system architecture and design.

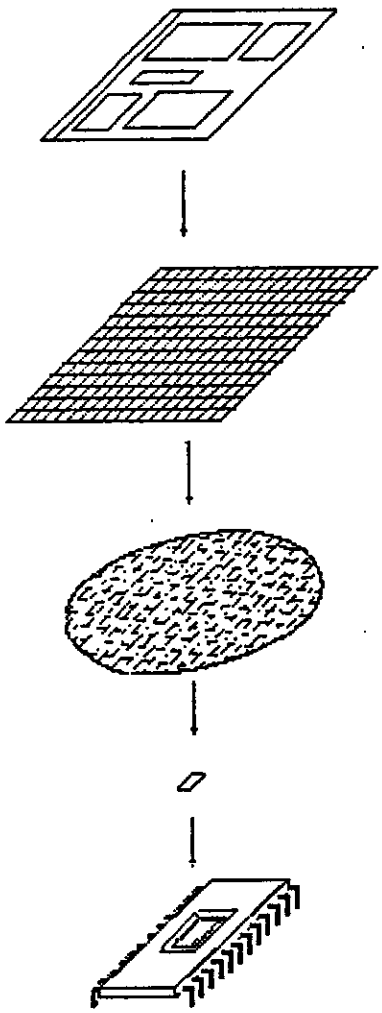
Acknowledgements

We wish to express our gratitude to all the folks who pulled together with us to make MPC79 happen, including our friends at Defense ARPA, at Micro Mask, and at Hewlett-Packard/ICPL. We all owe a great deal to the dedication and efforts of the instructors and lab coordinators in the universities, who, working under great pressure and on a tight schedule, have done such a fantastic job with their design courses and project-labs this fall. We especially want to thank all the student designers for their enthusiastic response to the courses, and for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well! Organizing and carrying out the implementation of these many imaginative VLSI design projects has been a very exciting and rewarding experience for us here at Xerox PARC/SSL.

MPC79 Flowchart:

DS 12; 9 PlaCell;
(5 Items.);
L NM; B L 4000 W 1000 C 2000, -750;
. . .
L NP; B L 500 W 4000 C 2500. -2000;
DF;

TO: MPC79@PARC-MAXC
FROM: REB@MIT-XX
SUBJECT: IMPLEMENT PROJ.CIF



USER COMMUNITY

~ 100 Designers at:
MIT, Caltech, Carnegie-Mellon Univ., Stanford,
Univ. of Illinois, U.C.Berkeley, Univ. of Wash., - - -
(using AIDS/LAP/ICARUS/etc..)

(MSGS, Design Files)

Project lab coordinators at each school use local electronic mail and file transfer facilities to interact with the designers and use the ARPANET to interact with MPC79

DATA COMM. FACILITY

(MSGS, CIF2.0 Design Files)

ARPANET
(MSG, FTP, TELNET)

(MSGS, CIF2.0 Design Files)

IMPL.FACILITY

INFO.MGMT SYSTEM: XEROX PARC/SSL
Checking, Planning, Merging of Designs into Starting Frames
Meeting of Constraints, Coordination , Logistics

(Constraints, logistics, control info.)

(Design files, merged into Starting Frames)

"The Foundry"

MASKMAKING: MICRO MASK, INC.
Data format: MEBES; ETEC electron-beam system

(MASKS)

WAFER FABRICATION: H-P/ICPL
NMOS Silicon Gate
LAMBDA = 2.5 MICRONS

(WAFERS)

PACKAGING

(Bonding Maps) (Packaged Chips) (Elect. Params) (Plots)

Packaged Chips, custom wire-bonded per project, along with plots, wire-bonding maps, and results of electrical testing, to send back to the designers for functional testing.