4. Starting Frame Documentation

The following pages describe the structure, function, and use of the various objects in the MPC580 starting frames (a starting frame is the set of all those layout artifacts, not associated with any particular design project, which serve to convey a project chip through maskmaking, wafer fabrication, and electrical testing). Included are the die dimensions and layout, the scribe-line profile, and descriptions of the alignment marks, layer codes, critical dimension testers, etch test patterns, die identification codes, discrete test transistors, ring oscillator, test resistors, contact tester, layer tester, and die code-letters. We used two different starting frames for MPC580. One was used for the first 4 runs which all had the same, relatively small die size. The second was used only on the 5th run which had a relatively large die size to accomodate the larger projects.

Die Dimensions and Layout

As in the Mead & Conway LSI design philosophy, it is wise to anticipate future miniaturization by parametering the absolute sizes of things. We parameterize the starting frame somewhat by representing the overall die length as L and the overall die height as H.

Overall Die Dimensions: L x H microns

MPC580 dies A,B,C,D:	6350 x 6350 microns	(250 x 250 mils)
MPC580 die E:	6350 x 8686 microns	(250 x 342 mils)

The starting frame dimensions are:

Vertical		Horizontal	
Scribe-Line Profile:	77 microns.	Scribe-Line Profile:	77 microns.
Setback:	21 microns.	Setback:	21 microns.
Universal patterns:	370 microns.	Maximum project:	H−196 microns.
Setback:	20 microns.	Setback:	21 microns.
Maximum project:	L−586 microns.	Scribe-Line Profile:	77 microns.
Setback:	21 microns.		
Scribe-Line Profile:	77 microns.		

Maximum Project:

MPC580 dies A,B,C,D:	5764 x 6154 microns	(227 x 242 mils)
MPC580 die E:	5764 x 8490 microns	(227 x 334 mils)

Scribe-Line Profile.

The scribe-line makes it easier to cut the wafer into dice. The scribe-line profile includes the scribe-line itself and two guard bands of poly and metal. The scribe-line itself is a coincident diffusion, contact cut, and overglass cut, 55, 53, and 40 microns, respectively, to either side of center. This removes all oxide, allowing the wafer saw to cut directly into the silicon wafer. Overlapping the edge of the diffusion by −10 to +8 microns is a band of polysilicon. Seven microns from the diffusion in the scribe-line is a 15-micron-wide band of metal which serves as a visual guide to the saw operator and separates the project area from the saw area.

Alignment Marks.

Two kinds of alignment marks are provided. In the upper left corner of the die is a square appearing on all layers; this provides a gross alignment indicator. For fine alignment, to its right are a sequence of "Squares" and "Fortresses" as described in Section 6.1 of the Xerox PARC/SSL

Report, *A Guide to LSI Implementation*, 2nd edition, by Hon & Sequin (Sect. 7.1 in 1st edition).

Layer Codes, Critical Dimension Testers, and Etch Test Patterns (Ells)

Below the alignment marks appears a set of six similar patterns, one for each of the six layers. Each consists of three items: the layer code {DIF, IMP, POL, CUT, MET, or PAD}, two critical-dimension crosses, and a set of L-shaped etch test patterns.

Critical Dimension Testers are two crosses with line widths of two lambda and as follows:

DIF	2 lambda	CUT	2 lambda
IMP	4 lambda	MET	4 lambda
POL	2 lambda	PAD	4 lambda

Etch test patterns (ells) are 26 lambda high. Smaller ells, with one lambda width and spacing, are nested inside the upper right corner of larger ells with two lambda width and spacing. In addition, there is a vertical two-lambda-wide bar down the left side of the pattern to make measurement easier.

Although digital stretching of various layers may be specified for all active devices, no stretching is performed on critical dimension testers and etch test patterns.

Identification Code

Each die has a unique seven-character identifier, *e.g.* "MPC05AF". The first three characters "MPC" indicate that this is a Multi-Project Chip. The next two characters indicate the year and month, respectively; *i.e.*, '0'=1980, '5'=May. The next two characters indicate the wafer and die, respectively. For example, letters "MPC05AF" indicate that this is die type F on wafer type A.

Discrete Test Transistors

Discrete devices are shown for measurement of dc parameters such as threshold voltages. Figure 1 shows the location within the starting frame and pad connections for the test devices.

Four devices, with sources and gates are bussed together, but having separate drains, are provided. All have four lambda wide by two lambda long channels. There is one device of each of the following types:

Metal gate, field oxide.
Poly gate, field oxide.
Poly gate, thin oxide.
Poly gate, thin oxide, ion implant (depletion mode),

Ring Oscillator

The ring oscillator is used to estimate the speed of devices made using this process. It consists of nineteen identical inverters in a circle, and a twentieth as a buffer to drive a line to a standard output pad, where there is more buffering to drive the outside world. Each inverter in the circle is minimum geometry, K=4. Pulldowns have four lambda wide by two lambda long channels. Pullups have two lambda wide by four lambda long channels. Since the oscillator period T equals the delay twice around the loop, the inverter pair delay is T/n, where n is between 19 and 20 since eighteen of the inverters drive only one similar inverter but the nineteenth drives two.

Test Resistors

There are two Van Der Pauw structures, one in polysilicon and one in diffusion, with identical geometry as shown in Figure 2. In a Van Der Pauw structure, there are two pads at each end of each resistor to allow separate current feed and voltage sense paths to the layer being tested, so that probe and contact resistance does not introduce error into the measurement. These devices provide a long aspect ratio (266.5 to 280.5 squares, depending on how corners are treated*) path of

minimum width (two lambda). Because of edge effects, sheet resistivity estimates from these measurements (sheet resistivity = total resistance divided by aspect ratio) are only approximate for other than two lambda wide lines.

*For further information on paths that go around corners in sheets of resistive material, see D. Vitkovitch, Ed., *Field Analysis, Experimental and Computational Methods*, D. Van Nostrand Co., Ltd., 1966.

Visual Identification

The wafer and die code letters, 370 microns (15 mils) tall, are repeated in the upper right corner of the die, for visual identification. Good eyesight and strong light are needed.

MPC Starting Frame Test Devices

Transistors

1 Drain, metal gate, field oxide
2 Drain, poly gate, field oxide
3 Drain, enhancement mode
4 Drain, depletion mode
5 Source (common)
6 Gate (common)

Ring Oscillator

1 Scribe line
2 Scribe line
3 Scribe line
4 Vdd (+5v)
5 Output
6 Ground

Resistors

1 Poly end
2 Poly end
3 Center
4 Center
5 Diffusion end
6 Diffusion end