1. Introduction and Overview

This introductory section provides background information about MPC580. Summaries are provided of the participants, of the organizations involved in the implementation effort.

Section 2 contains important basic information that the designers can use to prepare the chips for testing. Section 3 contains a complete list of all projects and designers. Sections 4 and 5 provide information about the starting frame and electrical test results. Finally, Section 6 discusses our plans for packaging and distributing more chips, and for distributing chip photographs.

The Background and Context of MPC580

Early in 1980, a new group, VCI (VLSI Computer Integration) was formed within the Systems Science Laboratory (SSL) at the Xerox Palo Alto Research Center (PARC). This group has several missions. Two of these are:

a) To help the external to Xerox community get MPC services for 1980.

b) To transfer the support of the ARPA sponsored university MPC services to an ARPA contractor - specifically USC-ISI (University of Southern California, Information Sciences Institute).

The Participants in MPC580

The user community for this multi-project chip set was composed primarily of EE/CS students taking courses in VLSI system design at major universities throughout the United States, along with a number of university faculty and research staff members undertaking major VLSI system designs. In addition, ARPA sponsored a few non-university organizations.

The MPC580 chip set contains a total of 171 VLSI system design projects from a total of 15 participating organizations. Designs were included from BBN (Bolt Beranek and Newman, Inc.), Caltech, CMU, ISI, JPL (Jet Propulsion Laboratory), M.I.T., Stanford University, Univ. of California at Berkeley, UCLA, Univ. of Colorado, Univ. of Illinois, Univ. of Rochester, USC, Washington Univ. at St. Louis, and a few test patterns and "pictures" from Xerox PARC.

Organizations involved in the implementation effort

Several other organizations collaborated closely with us: Data communications (electronic messages, design file transfers) were supported using the ARPANET for the ARPA supported organizations - the GTE Telenet for the Xerox supported organizations; wafer fabrication was done by Hewlett-Packard's Integrated Circuit Processing Laboratory; ISI helped us substantially with the reading and writing of magnetic tapes and with some of the preparation of this document; maskmaking was done by Micro Mask, Inc., using an electron-beam maskmaking system; and packaging was done by Systems Concepts Inc utilizing equipment at Xerox PARC's Integrated Circuits Lab.

For an overview of the flow of information and artifacts through these various organizations, see the MPC580 Flowchart at the end of this section.

MPC580 implementation schedule and details

MPC580 had a scheduled project submission cutoff time of 1700 PDT on May 30, 1980. We attempted to run MPC580 as a spooler with new project requests being accepted as early as April 15, 1980 and implement requests being accepted as early as May 1, 1980. What actually happened was an enormous surprise to us. Virtually everyone waited until the last minute. Undoubtedly people were checking designs as carefully as they could before final submission for implementation. The pace on May 29 and 30 was quite frantic for us as we tried to keep up with the requests. Unfortunately, we had some hardware reliability problems with the PARC-MAXC computer which had us off the net for approximately a 9 hour period in the last 24 hours of MPC580. We informally extended the deadline to approximately 2200 on May 30. The valiant efforts of Alan Bell, Kevin Gillette, and Maureen Stone during those final frantic hours were invaluable to the successful completion of MPC580. Ted Strollo finally shut down MPC580 at 2252 PDT on May 30. Each project coordinator was sent a copy of his/her status file.

When we finished, there were 4 projects that were in the open but not ready state. One of these was an initial handshake, a test file transmission not intended to be implemented. The other 3 were projects for which we received new project requests but no further messages. Since none of the project coordinators has told us we missed anything, we are assuming these 3 just didn't get any further into the pipeline than getting an ID assigned.

With MPC580 we experimented with offering designers 2 values of lambda, 2.5 microns and 2.0 microns. Most projects (in fact all those in the first 4 wafer runs) were done at lambda of 2.5 microns. A few projects required the smaller value of lambda of 2.0 microns for either circuit size or speed considerations. These were implemented on the MPC580 5th wafer run.

Micro Mask and Hewlett-Packard gave us astonishingly fast turn around. MPC580 filled up 5 (FIVE) mask sets as compared with 2 (TWO) for MPC79. Micro Mask had early masks for us on 11 June 1980. All of the remaining masks for the first 4 runs were at HP within a week from that date thus HP was able to begin pipelining all 4 wafer runs. HP expects to have the first wafer runs back to us the week of July 7. We plan to ship packaged chips out of PARC the week of July 14. At this writing, we are not finished with all the fab/packaging/shipping cycle (The final set of masks for the fifth run which is lambda of 2 microns was delivered to HP June 30) but we expect it to be completed by approximately the end of July 1980.

Looking Ahead

The demand for VLSI implementation services will clearly increase. We are pleased to be part of the technology transfer of this service to ISI for the ARPA sponsored sites. There will be another run (tentatively scheduled for cut off January 30, 1981). With this run, the electronic mail and file transfers will be direct to ISI with Xerox assisting in the overall coordination of the effort.

Acknowledgements

We wish to express our gratitude to everyone who pulled together with us to make MPC580 happen, including Defense ARPA, ISI, Micro Mask, Hewlett-Packard/ICPL, Systems Concepts Inc, and Xerox Corporation for being so supportive of the effort. We all owe a great deal to the dedication and efforts of the instructors and project coordinators in the universities and

participating organizations, who, working under great pressure and on a tight schedule, have done such a fantastic job. We especially want to thank all the designers for their magnificent efforts and accomplishments on their VLSI system design projects. You have done well, and it has been our pleasure to serve you.

A Dedication

As organizer of MPC580, I, Ted Strollo, am dedicating the MPC580 project to Bill Plummer whose picture actually got imaged in the unusable for circuits area of the metal layer on wafer set D*. Bill provided the inspiration for a few fun hacks during MPC580, and, were it not for the fun and enjoyment I got out of those hacks, I might never have made it through to the completion of this effort. Many thanks to you Bill, you made it all worth while!

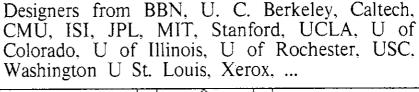*A picture of Alan Bell also got similarly imaged on wafer sets A,B, and C

MPC580 FLOWCHART

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(symbol PLACONNECT);
DS 42 250 10;
L ND; W 20 35,0 80,0;
...
L NM; W 40 35,-75 35,75;
DF;
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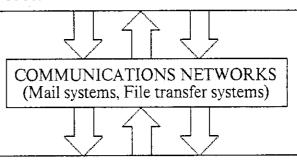
TO: MPC580@PARC-MAXC
FROM: COHEN@USC-ISIB
SUBJECT: IMPLEMENT MORSEISI

Designers from BBN, U. C. Berkeley, Caltech, CMU, ISI, JPL, MIT, Stanford, UCLA, U of Colorado, U of Illinois, U of Rochester, USC, Washington U St. Louis, Xerox, ...
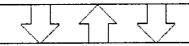
Project lab coordinators at each school use local electronic mail and file transfer facilities to interact with the designers and used the ARPANET and GTE TELENET to interact with MPC580.

COMMUNICATIONS NETWORKS
(Mail systems, File transfer systems)

Information Management: Xerox PARC/SSL
Checking, Planning, Merging of designs into starting frames
Meeting of Constraints, Coordination, Logistics.

Mask Making: Micro Mask Inc.
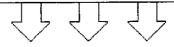Data format: MEBES; ETEC electron-beam system.

Wafer Fabrication: Hewlett-Packard/ICPL
NMOS Silicon Gate
LAMBDA = 2.0 and 2.5 microns

Packaging
Systems Concepts Inc., using Xerox/ICL equipment

Packaged chips, custom wire bonded per project, along with plots, wire bonding maps, and results of electrical testing, to send back to the designers for functional testing.