NORCHIP, a silicon brokers model

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Abstract. A Nordic Multi-Project-Chip organization with 26 design groups and 22 follow-up groups from five Nordic countries is described. The model for cooperation, the economy of the project, the applied technique and the impact on both industry and university research are dealt with. So far, 70 designs in three runs have been completed and 9 runs with 200 designs with extensive use of cell libraries are under way in 1983.

Aiming towards submicron technology MPC might be the only possible way for smaller companies and universities to have circuits made.

Keywords. Multi-Project-Chip, MPC, silicon broker, cell library concept.

1. Introduction

The breakthrough of VLSI technology is expected to have a strong impact on electronics industry. In the Nordic countries with smaller companies this calls for especially powerful methods for making the technique available to as many people as possible in industries and at universities, for education, research and

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prototyping. NORCHIP or the Multi-Project-Chip (MPC) approach, as introduced among others by Mead and Conway [1] and Craig Mudge [2] is one such method. We therefore started a joint Nordic MPC project with the goal to make LSI/VLSI technology easily available to industries, institutions and universities in the Nordic countries. Our task is then to provide our 'customers' with design rules and design handbooks and to take care of their designs by accepting layout descriptions on magnetic tape. We will then combine several designs into Multi-Project-Chips, have the chips manufactured by commercial fabrication lines and return bonded devices to the 'customers'. The aim of this project is to improve the MPC concept from an experiment to industrial environment.

2. NORCHIP organization

2.1. Participants

NORCHIP [3] was initiated by two technical universities in 1982 with Nordforsk, the Nordic Cooperative Organization for Applied Research, as administrative body. NORCHIP is directed by a board with elected representatives from the participating countries (see Fig. 1).

During 1982, 12 companies and institutions participated in the project. Now

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His actual field of research is the design of integrated circuits, computer-aided design, and design methodology.

He is chairman of the NORCHIP Board, and a member of the program committee for The European Solid State Circuit Conference.

Dr. Olesen is member of the board of the Danish Engineering Society and member of IEEE.

Christer M. Svensson was born in Borås, Sweden, 1941. He received the M.S. and Ph.D. degrees in Electrical Engineering from Chalmers University of Technology, Göteborg, Sweden, in 1965 and 1970 respectively.

He has been working with the Research Laboratory of Electronics III at Chalmers University as a teacher and scientist from 1965 to June 1978. In 1972 he was a guest scientist at the Jet Propulsion Laboratory, Pasadena, CA, U.S.A. He has performed research and development on MOS transistors, MNOS memory devices, Pd-MOS gas-sensitive transistors and the physics and chemistry of the MOS system.

Since July 1978 he is with the Department of Physics and Measurement Technology, Linköping University, Linköping, Sweden, first as a lecturer of applied physics, and, since November 1983, as professor of electron devices. In Linköping he continues the work with MOS physics but has also started a new research group on integrated circuit design, dealing with CMOS circuit techniques, CMOS system on chip and computer aided design.

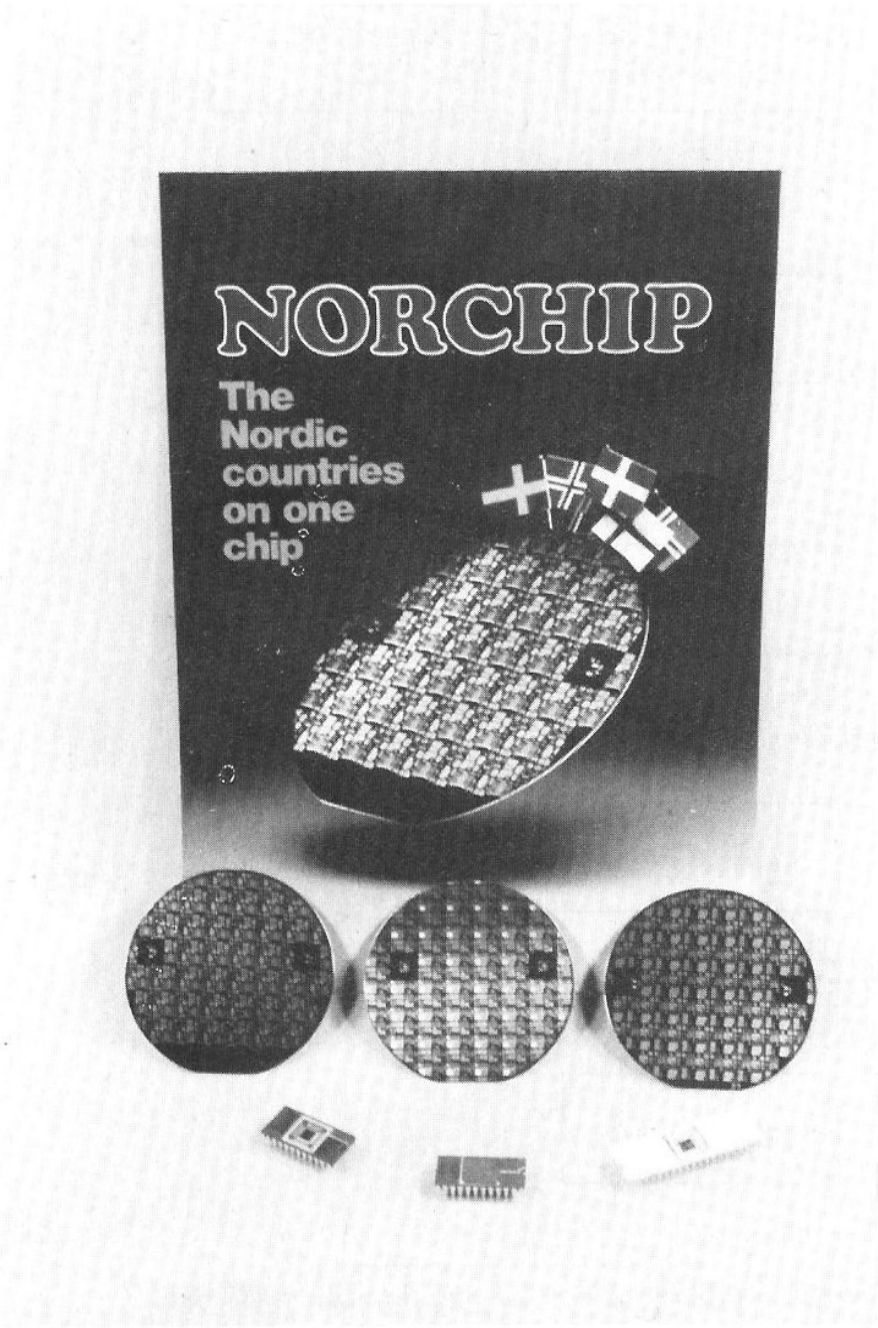

Fig. 1. Three runs with about 70 designs were completed during NORCHIP82. Process ASEA-HAFO, CMOS metal gate [2] and Hughes Microelectronics, Scotland [1]. Chipsize 10×10 mm^2.

there are 26 participating groups: 10 industrial companies, 6 service institutes for industry and 10 universities. Besides this a group of 22 industrial companies follows the project as potential new partners. The production scheme is shown in Fig. 2.

The NORCHIP board is responsible for economy and for negotiations with mask houses and wafer foundries. Regarding special job functions, Sentralinstitutt-tet for Industriell Forskning, Oslo, takes care of the editing on a CALMA-system. Linköping University delivered CMOS-metalgate cell libraries [4]. Electronics Institute, Technical University, Lyngby is responsible for administration of usergroup for cell libraries [5]. This includes both the design of new cells and buying available cell libraries.

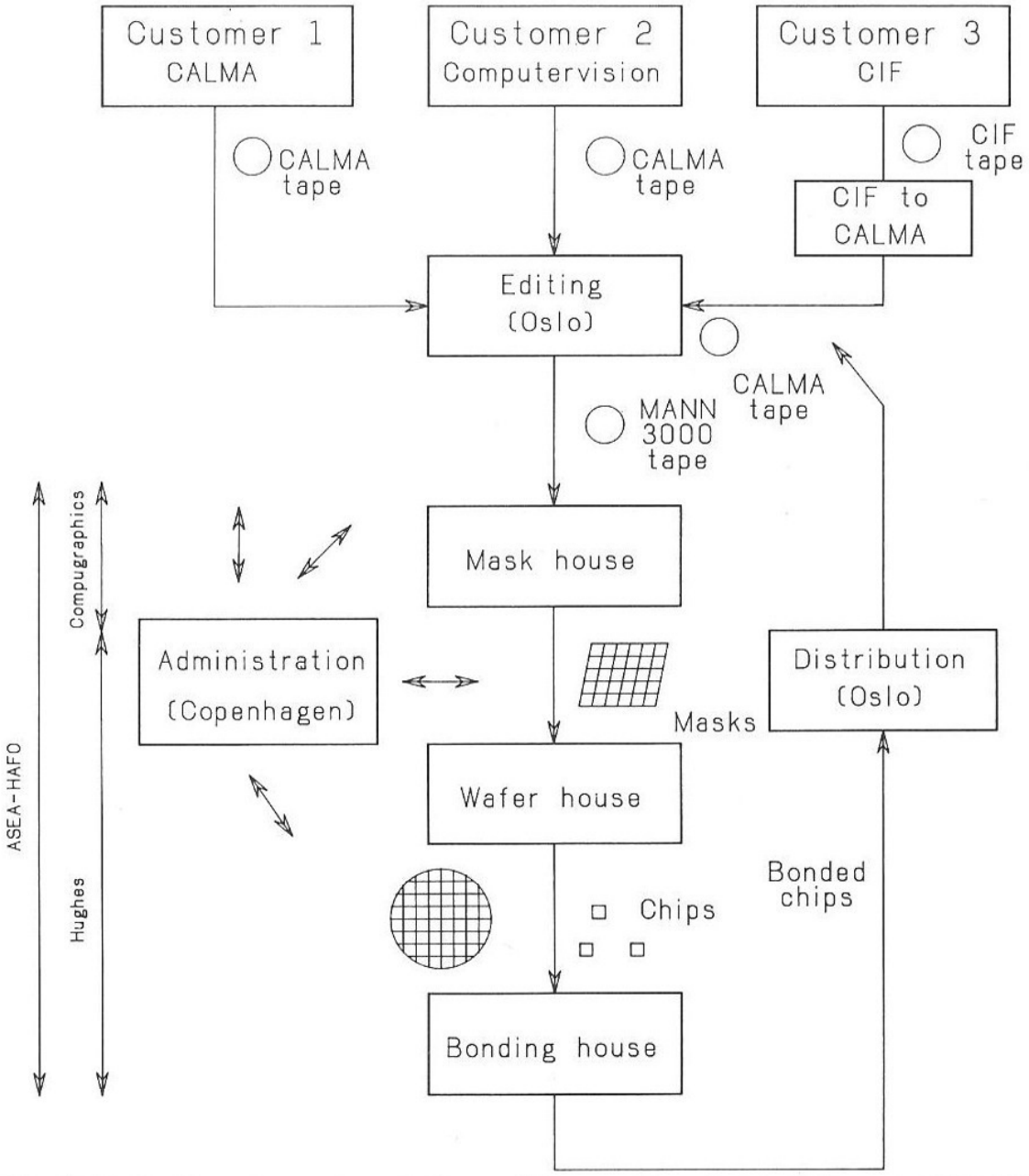

Fig. 2. Production scheme from design to delivery of bonded chip through NORCHIP.

2.2. *Economy of NORCHIP*

The NORCHIP pilot project in 1982 was completely funded by Nordisk Industrifond and the four national funds to get started. Now the funding only covers participation from institutions and some of the administrative jobs; this means that nearly 50% is paid by industry. Only expenses related to the wafer foundry business are funded. The design cost is paid by the participants.

The idea behind the project is to share the costs of masking and wafer processing. The prices per run with 10 4″ wafers are about US $18 000. With our standard chip size of 10×10 mm^2 this means US $180 per mm^2. A typical chip of 4×4 mm^2 would then cost $4 \times 4 \times 180 =$ US $2880. For this amount you get 10 bonded samples and with 10 4″ wafers a total number of 10×50 chips are available for bonding. This price is less than one fifth of the price for processing

one single circuit. The mask making is the most expensive part of the deal. Besides the economic advantage the customer is free from all negotiations with the mask house and wafer foundry.

3. Status of NORCHIP

3.1. Interface to all design systems

The 26 design groups in NORCHIP have a variety of design systems from advanced integrated design systems to 'home made' systems, based on CALMA, Computervision, VAX, IBM, CIF, LAP and Lucie. The first job in the project was to interface them to the CALMA format. The CIF to CALMA translation was done in Linköping University. The Technical University of Stockholm made a CALMA format from their LAP-program. Lucie still needs a CALMA system to get the data transformed to CALMA.

3.2. Interface to mask house and wafer foundry

The most difficult task was to get the right interface and a reasonable contract with the mask house and wafer foundry because they need volume of course and their willingness to do foundry business depends on the economic situation. NORCHIP negotiated with 3 mask houses and 9 foundries to obtain reasonable service. The selected mask houses were ASEA-HAFO (Sweden) and Compugraphics (Scotland). The wafer foundries were ASEA-HAFO (Sweden), Huges Microelectronics (Scotland), Vaisala (Finland) and AMI (CA, U.S.A.). In addition, SAAB-SCANIA (Sweden) is used as second source for bonding.

The crucial point in those negotiations is to get all necessary information from the foundry to secure the success of the project. As foundry business is relatively new, no standards have been established yet. In this respect, NORCHIP can break new ways. The critical points are sufficient documentation on design rules, cell libraries and test chips. Another critical point is time of delivery. Without a solid organization and some production volume included it would be difficult to solve those problems. To get second source, appointments are made to make design rules and masks compatible for two foundries.

3.3. Three 10×10 mm^2 NORCHIP's run during 1982

The main interest in NORCHIP has been CMOS technology. Two runs in metal gate CMOS technology with 6 μm design rules have been completed with ASEA-HAFO. One run in iso CMOS technology with 5 μm design rules has been completed with Hughes Microelectronics.

The first run (NORCHIP1) thus used a metal gate process with design rules recommended by NORCHIP. Design rules and other information ('design handbook') was destributed as a report, "A CMOS design manual" [4]. Also a

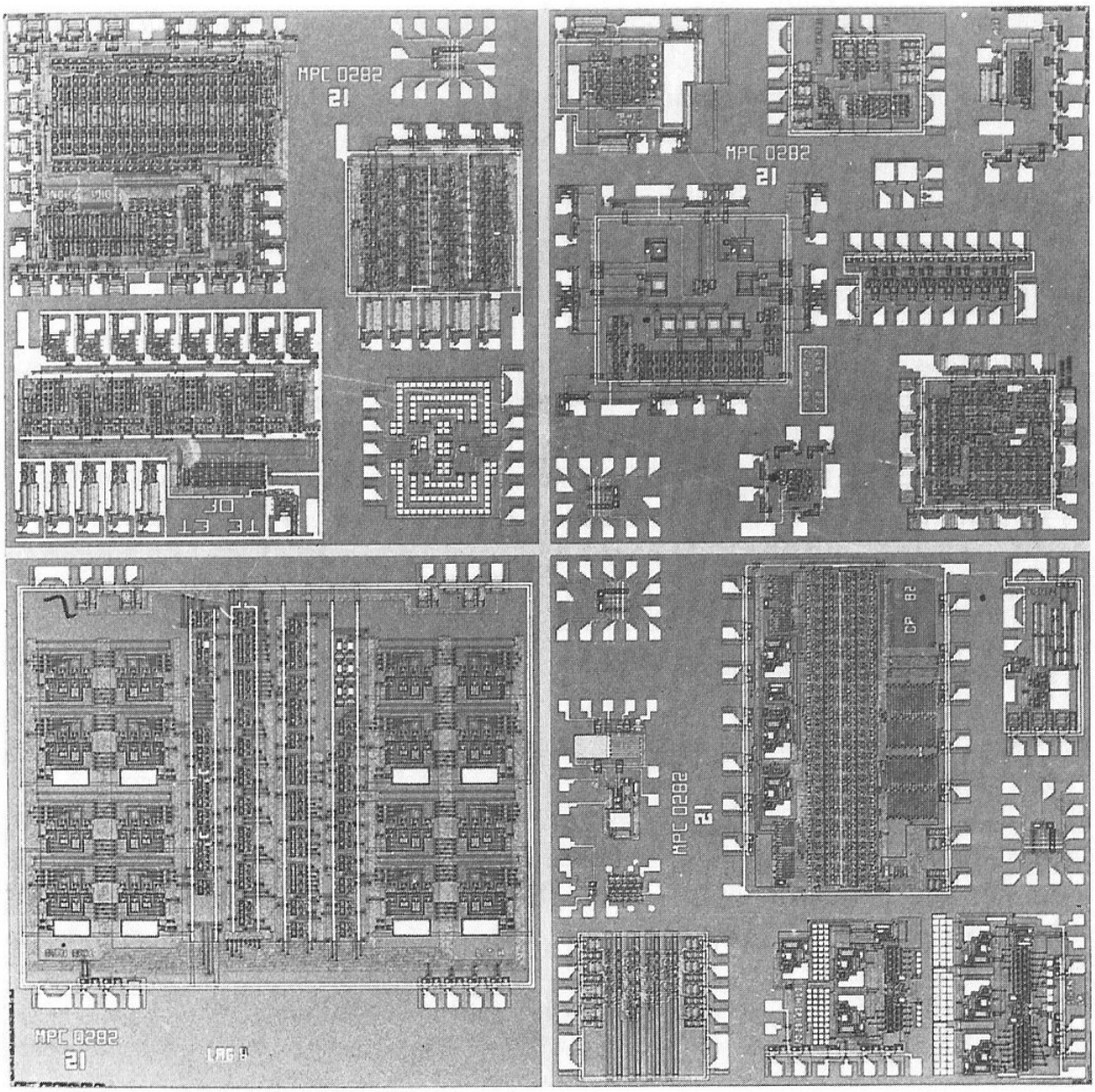

Fig. 3. NORCHIP1 with 15 designs in metal gate CMOS from 10 different groups in Denmark, Finland, Norway and Sweden. Chipsize 10×10 mm^2.

small cell library was available from NORCHIP. The chip included 15 designs from 10 different groups in Denmark, Finland, Norway and Sweden. It was fabricated and delivered in 4 months. Each participant received 10 bonded chips. A chip photograph is shown in Fig. 3.

The second run used iso CMOS technology from Hughes Microelectronics. Design rules from [4] or from Hughes could be used. Detailed design rules and SPICE simulation data from Hughes was distributed to the participants. This first iso CMOS run was unfortunately delayed due to processing problems and delivered first in June 1983. The third run again used metal gate CMOS and was again delivered in 4 months.

3.4. Some results from the first runs

NORCHIP1 contained analog, digital and mixed circuits including switched capacitor filters and A/D and D/A converters, designed by universities, industries and other institutions. Because of lack of proper testing of the chips by NORCHIP, we discovered rather late that some process parameters were just outside acceptable values. This caused malfunction of many analog designs, but the digital ones still worked. The chip was refabricated by our vendor and new chips delivered in early spring 1983.

Let us mention some examples of successful designs from this first chip. Linköping University (Sweden) submitted a digital circuit for memory managing in a digital signal delay system [6]. This circuit is now in use in a hearing aid prototype. A simple shaft encoder circuit was successfully designed at Chalmers University (Sweden) [7]. The circuit was then further developed (with on chip photodiodes) for NORCHIP3. Lohja Elekktroniikka (Finland) has developed a circuit to be used in an electroluminescent display driver which was successfully rerun in NORCHIP 1.

3.5. Postprocessing of MPC-sensors on chip

Several projects on NORCHIP1 concerned sensors on chip. In these cases we still use the full standard CMOS process (together with all other chips), but the 'customer' makes some processing in his (her) own laboratory. One example of such a project is the integrated heat radiation detectors developed by the National Defense Research Institute (FOA) in Sweden. In this circuit all logic and signal processing are done in standard CMOS technology whereas the heat radiation detectors are made by wafer postprocessing. In postprocessing, palladium silicide schottky detectors are fabricated in preprepared areas. All CMOS circuitry worked on this chip but postprocessing is not yet finished.

3.6. Some practical conclusions from NORCHIP82

The experiences from NORCHIP82 are mainly very positive. We have demonstrated that a project of this type can be run by limited resources and no new investments. We have demonstrated our ability to simultaneously handle designs from many different groups using different design systems and different design rules. We have demonstrated that many people, at universities or in industries, can quite easily get involved in 'full custom' design work. We have also found that the regularity in NORCHIP runs is very valuable as our 'customers' easily can redesign and refabricate circuits with design errors. They can also develop and test several subsystems in one run and a whole system is the next.

Of course we have had some problems also. We have learned that we need a better control of chip quality. NORCHIP should take a more active role in testing testchips and in visual inspection. We have also learned not to use a fresh process, but to concentrate on well-established processes. We should try to reduce the present 4 month of turnaround time.

We have found that the national electronic research institutes, Elektronisk Institut (Denmark), Sentralinstitutt for Industriell Forskning (Norway) and VTT (Finland) have been very important for spreading NORCHIP to medium size or smaller industries. These institutes have made design systems (CALMA or Computervision) available for external customers. In Sweden we have been less successful in reaching the medium size or smaller industries due to lack of an electronic institute.

3.7. NORCHIP83 under way

Based on the success of the NORCHIP pilot project during 1982 the 83 project has started with plans for 9 runs including up to 200 smaller and larger designs. As some of the groups in NORCHIP82 were relatively new in the field of LSI design, the complexity of the circuits is growing very fast as experience and improved tools are available. The tools are, besides CAD-tools, the base of cell libraries and earlier designs. We also expect a larger part product oriented circuits during 1983.

NORCHIP83 will also include a number of regular multiprojectchip courses. The first undergraduate MPC-course was given at Linköping University (Sweden) during fall 1982 and used an own chip in cooperation with NORCHIP (metal gate CMOS) [8]. A new course at the Royal Institute of Technology (Sweden) and the next year Linköping course will use NORCHIP. The first industrial MPC-course in the Nordic countries was given at the Royal Institute during spring 1981.

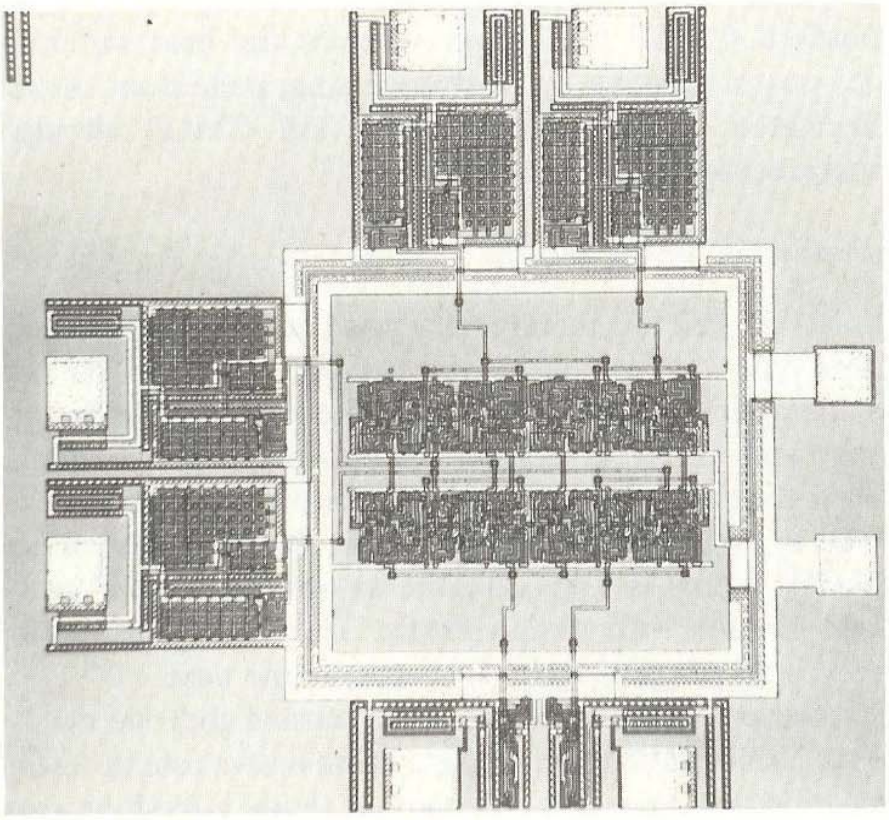

Fig. 4. Modular cell design with double cell height and four interconnectivety channels. Iso CMOS 5 μm design rules. Diagram Fig. 5.

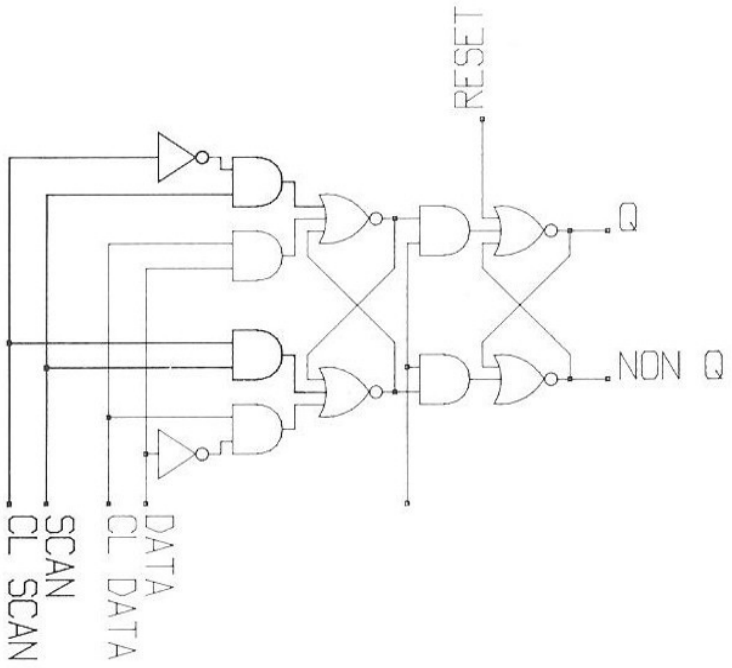

Fig. 5. Example of polarity hold device with Level Sensitive Scan Design.

Industrial courses are now given regularly (starting spring 1983) by SIFO, a Swedish Institute of industrial education, using NORCHIP.

4. The cell library concept

In all Nordic countries the gate arrays are widely used. It is easy to get started. Many companies are offering excellent service and the prices are reasonable for small volumes. Therefore, NORCHIP does not include gate arrays. The main effort is placed on standard cell and general cell libraries and mixed analog/digital designs. A separate project on administration of a usergroup for cell libraries has been set up. Until now a total of 143 cells are available for the participants [4,5]. This includes 36 cells from AMI iso CMOS 5 μm standard cells. Also efforts are made both to buy more cells and to design MSI-LSI cells including RAM's and ROM's and linear cells.

As some of the university groups are working on general routers and silicon compiler projects, this work is expected to be important as a start to faster and less error prone designs. It is very difficult to buy cell libraries. Some vendors prefer to sell only on symbolic form to secure that they will get the processing. In other cases you have to sign a contract that a certain percentage of the production will go to that company. In all cases there seems to be a lack of updated and well documented cells of reasonable complexity.

A systematic approach for cell design with modular structure, extensive use of extraction, checking, simulation and standardization has been set up to make both new design and redesign to new design rules very fast. Fig. 4 shows a cell with double cell height and LSSD for testability. Fig. 5 shows the schematic.

5. The future of NORCHIP

The MPC-concept in itself is not original as many universities have done it for years and every small company could start their own MPC today if they were interested. But to be respected by wafer foundries, to get some good deals, to get reasonable turnaround time with nearly montly runs, to get professional service etc., you need a strong organization to take care of your designs.

NORCHIP has reached a reasonable size with a calculated turn over a US $2 000 000 for 1983. We expect that if NORCHIP83 meets with reasonable success, a permanent NORCHIP organization run by the service institutes in a commercial frame will result. Some funding will still be needed for participation from universities.

We believe that sharing knowledge and experiences among industries using customer designed circuits is a very important way towards success. We hope that NORCHIP will be able to contribute to this, by being a natural meeting place for all groups involved in customer designed circuits. The NORCHIP cell library effort, described above, is the first step towards this cooperation.

Another very important aspect on customer designed circuits is education. We believe that the most effective way to introduce new techniques in industry is through new engineers entering industry. Basic engineering education therefore plays a key role. We hope that it will be possible to make silicon area available to universities in our countries, for undergraduate courses, diploma works and thesis works. This should then be funded directly from the national university administrations and run through the NORCHIP organization.

Several new joint projects are formed among the NORCHIP participants to get a complete IC-line. The most relevant to mention is a project on test pattern generation for VLSI and a project on iso CMOS-processing all of which are supported by Nordisk Industrifond.

6. Conclusion

Even though VLSI is a very fast accelerating and very capital intensive technology, it has been proven that cooperation between univerisities, industry and even between countries can give good results for a modest amount of money. Entering the submicron age it is clear that on one side design systems will become relatively cheaper and more effective, while wafer processing will be more expensive and centralized. In the future, very few universities and small companies can afford to have a complete up-to-date process line.

Consequently, a project like NORCHIP can break new ways of thinking in improving and standardizing the interface between designcenter and wafer foundry and in proving that MPC is not only a university game but can be run as a commercially attractive route for prototyping and small volume VLSI, more advanced and general than gate arrays. In this way, foundry business also becomes easier, and more attractive for the foundries.

Acknowledgment

We would like to thank the other members of the NORCHIP board, Erik Carlsson, Marcus Bayegan, Helena Pohjonen and Erik Bornhoeft, for their valuable work. Hans Jonassen, Rolf Sundblad and Peter Østergaard Nielsen also contributed to the success of this project.

Note added in proof

The original paper was written in June 1983. Per February 1984 the following updates can be made.

The number of participants in the project has increased to 34 active member groups distributed over 14 industrial companies, 9 service institutes and 11 university groups. The follow-up group has increased to 33 members.

The number of 10×10 mm^2 designs completed is 10. As new mask house Microfab is included and AMI is included for wafer processing. As a first step in the commercializing of NORCHIP, general manager Oddvar Åserud, Nordic VLSI, Norway, will take over the coordination and marketing of the project. The project, however, is still headed by a board, and university participation is an important aspect of the project.

NORCHIP84 will include a minimum of 9 runs in mixed 5 and 3 μm ISO-CMOS technology. The highlights of the NORCHIP84 are wafer acceptance control, expanded activities on cell libraries, and tight control of turn around time.

In the new project, 'Multi Project Wafer' (MPW) will be adopted also to fulfill the need for chip size and more flexibility.

NORCHIP arranged a popular seminar in Finland, autumn 1983, where some participants presented their results and the foundries presented their new proposals.

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