Conference on Microelectronics
1982, Adelaide, 12-14 May

Australia's First Multi-Project Chip Implementation System

J.C. MUDGE
Head, VLSI Program, Division of Computing Research, CSIRO, Adelaide
and
R.J. CLARKE
Co-ordinator, VLSI Program, Division of Computing Research, CSIRO, Adelaide

SUMMARY A proven integrated-circuit design methodology, based upon the pioneering work of Mead & Conway, was introduced to Australia in 1981. This has led to a radical increase in the number of integrated-circuit designers.

To complement this, CSIRO has designed a chip implementation system for the rapid, remote fabrication of experimental designs. By combining the pattern-generation files of many independent designs to form one mask set, fabrication costs are reduced by an order of magnitude.

The components of the implementation system are (a) a standard interface to fabrication; and (b) information and logistics management. The first fabrication run will use electron-beam masks, a five-micron n-channel silicon gate process, and a forty-pin package.

1 INTRODUCTION

As the application of microelectronics becomes more pervasive, systems designers, who formerly constructed electronic systems from standard chips (often microprocessors), are now faced with designing complete applications systems on silicon.

A new training need has therefore arisen - the training of new electrical engineering and computer science students and the retraining of of practising designers (in industry and research laboratories). The pioneering work of Mead & Conway (1980) appears to be the most successful approach to solving the teaching need. Courses based on their work are now being taught at over a hundred universities in the United States; several such courses are being introduced in 1982 in Australian universities and institutes of technology.

This increase in design activity has created a demand for chip fabrication that is not met by the conventional manufacturers of chips ((i) firms who design and manufacture integrated circuits; and (ii) teaching and research institutions who own fabrication equipment for student use). The demand comes from both students (in training or retraining) and trained designers who wish to fabricate their prototypes.

The main steps in fabrication are mask making, wafer processing, and packaging. At each step, a designer faces both technical and logistics problems. A sample of these follows:-

1.1 Lack of Technical Specification

In the traditional integrated-circuit firm, chip designers and process designers sit side-by-side. Much technical information passing between the two groups is never documented, and yet mut be known by a designer.

1.2 High Variability Between Vendors

Different firms have quite different conventions (mask polarities, for example), process tolerances, and electrical performance. Even such fundamental electrical parameters as transistor-threshold voltages vary from vendor to vendor.

1.3 High Costs

Although a designer needs only a few chips to test his prototype design, he must pay for the set-up costs and processing of a complete batch run (of around 1,000 chips). Prices range from $30,000 to $50,000 for such a run.

1.4 Vendor Interface Logistics

Because some of the steps, mask making for example, must be done overseas, the problem of communication is exacerbated by geographical distance and international boundaries. Not only must very detailed and sophisticated technical detail be exchanged, but export licences and customs clearances are required. The problems of logistics deter all but the naive designer.

1.5 Unpredictability of Turnaround Time

Because the designer of applications systems offers only a low-volume business to a semiconductor manufacturer, his run is likely to be pre-empted by high-volume designs. This is particularly true of university designs; delays of up to twelve months have been observed, with four months being the common delay through all of the queues.

Clearly, an implementation system is needed which

a. presents, to the designer, a standard technical interface to manufacture;

b. reduces the cost;

c. simplifies the logistics.