DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS 02139

To: EE/CS department faculty, staff, and students.

From: Lynn Conway, 36-595, X3079.

As a part of course 6.978, a series of seminars concerning VLSI computer system architecture will be held on Dec. 5, Dec. 7, and Dec. 8, as listed below. You are invited to attend.

"Highly Concurrent Systems",
Carver Mead,
Prof. of Computer Science, Electrical Engineering, & Applied Physics,
California Institute of Technology.
Tuesday, Dec. 5, 1:30-3:00, Rm 39-400.

"Recursive Machines: A non-von Neumann VLSI Architecture",
Wayne Wilner,
Member of the Research Staff,
Xerox Palo Alto Research Center.
Thursday, Dec. 7, 1:30-3:00, Rm 39-400.

"Project X-Tree". (see attached abstract),
Carlo Sequin,
Assoc. Prof. of Electrical Engineering and Computer Science,
University of California, Berkeley.
Friday, Dec. 8, 3:00-4:30, Rm 39-400.

6.978. SEMINAR DEC 7

"Recursive Machines: A non-Von Neumann VLSI Architectures".

- undergraduate work at M.I.T.
- earned the Ph.D. in computer at Stanford working under Don Knuth.
- ~~[illegible]~~ Computer architect particularly Burroughs, one of the architects of the B1700.
- Now mem. Res Staff at PARC, Doing some very innovative work in Computer Architecture.
- The Subject of his Seminar is:

- Projects all successfully transmitted to PARC, successfully merged into ICARUS design file. Now being conv. to PG format and checked --- then on to maskmaking. I'll keep you informed of progress.

6.978 SEMINAR

This is the third in a series of Seminars this week on the subject of VLSI Computer System Architecture.

It is a real pleasure to introduce today's speaker:

Prof. Carlo Séquin of the
Dept of EE & CS at
University of California, in Berkeley

- Carlo earned his Ph.D in Physics at the University of Basel, in Switzerland.
- He then joined Bell Labs as a Member of the Tech. Staff, in the early 70's and was one of the Pioneers in Charge Transfer Devices, such as CCD's. Carlo is the senior author of a text on that subject.
- In 1977, he joined the Faculty at Berkeley, and has since been very actively involved in both research and teaching in the area of very large scale integrated systems.
- The subject of Carlo's talk today is Project X-Tree.

Carlo ---

Criticisms:
- <u>Snyder's</u>: Address Need Question as trees are merged.
- <u>Corby's</u>: " " as trees deleted.
- <u>Levy/Bryant</u>: Deadlock loops in Fifo's.

PROJECT X-TREE

C.H.Séquin, A.M.Despain and D.A.Patterson

Computer Science Division
Electrical Engineering and Computer Sciences
University of California
Berkeley, California 94720

The question how future computing systems can best exploit the computational power of forthcoming VLSI components is studied. "X-tree" is one possible answer based on a modular approach in which the basic building block, "X-node" is a single-chip VLSI computer. An unlimited number of these components are organized into a binary tree, which is enhanced by additional links to provide fault tolerance and a more uniform message traffic distribution. This organization overcomes the communications bottleneck of traditional multiprocessor systems, while remaining within the constraints of the limited pin number of the single-chip components.

X-node itself consists of a dynamically microprogrammable processor, a two-level memory hierarchy and a communications switching network, all ulimately to be integrated on one or two high-density VLSI MOS chips. The project is at an early stage of research. The construction of prototypes of the link between nodes and the communications parts of X-node have been started.

Interconnection topology, addressing scheme, routing algorithm, message format and tentative ideas on switching hardware and the architecture of X-node will be discussed.