SEMINAR: NOVEMBER 21

ON BOARD: 6.978. TODAY: SEMINAR BY RICHARD LYON, M.R.S. XRPARC "VLSI IMPLEMENTATION OF SPEECH PROCESSING FUNCTIONS".

- First: Project Info / Status: If you have plots or more details on your project - hand in after Seminar.
- A number of projects are far enough along to be likely candidates for implementation. Please keep me informed of your exact bounding box dimensions as you determine or change them. I'm building a tentative map of the project chip.

- I'll begin allocating space on the chip starting early next week. If you want to put your project on the chip, see me, show me evidence of your progress, and size of project. Late next week we'll send preliminary files to PARC for plotting - getting the plots back here for checking. Final Design files should be ready ~ 5 December.

- ~~Be prepared to get new versions of library cells no dimensional or connection point changes - just that we might find sight errors ---. We'll firm this up next week.~~

- Digitize so that Box centers and edges fall on 1/2 micron grid and no finer. i.e. numbers in centimicrons should end as --- 50.

- I'll be in today & tomorrow. I'll be away during thanksgiving. If group want to use 1-6 - organize and see me tomorrow for key.

- Note: My home # is 494-8188. During next few weeks feel free to call me at home about projects -- questions, info, status, etc.

- WE'VE TESTED THE ARPANET FOR SHIPPING FILES TO PARC -- & HAVE PLOTS BACK FOR PIECES OF DESIGNS BY 6-7 STEELE, RICHARD STERN, STEVE FRANK.

TODAY: I'm very pleased to introduce Dick Lyon, who is a Member of the Res. Staff at Xerox PARC.

Dick is Xerox Corporation's Principle Investigator in the areas of Speech and Signal Processing.

His subject Today:

"VLSI Implementation of Speech Processing Functions"

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

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Memorandum

To: The IC Group (and others interested)

From: Lynn Conway

Subject: Seminar Announcement

On Tuesday, November 21, from 1:30-3:00 p.m. in room 39-400, Richard Lyon, Member of the Research Staff, Xerox PARC will be giving a seminar titled:

VLSI Implementation of Speech Processing Functions

Abstract:

The cost of implementation of special-purpose signal processing hardware has been rapidly decreasing in recent years under the influence of new technologies. Very Large Scale Integration now enables the design and construction of digital filters and other signal processing structures at costs low enough to spur an applications revolution.

At Xerox PARC, speech recognition has been the motivating application for the development of several new integrated subsystems for speech processing. The predicted low replication costs for VLSI systems has had a major impact on the design of the speech processing algorithms, and on the architecture and design of the integrated hardware subsystems which implement the algorithms.

An overview of the Xerox PARC speech recognition project will be presented. The design of some of the integrated speech processing subsystems will be described, including the design of a single chip digital filterbank and its on-chip memory subsystem.