6.978 LECTURE #7. TUESDAY OCT 3

TODAY: SOME MORE CIRCUIT & DELAY CALCULATIONS WHICH AFFECT LAYOUT GEOMETRIES ··· SYST. DESIGNS

(i.e., NOW THAT YOU KNOW WHAT LAYOUT IS LIKE, YOU SEE WHY ITS A GOOD IDEA TO HAVE THINGS IN ORDER AT THE HIGHER LEVELS BEFORE COMMITING TO ALL THAT WORK !!!)

THURS: SUBSYSTEM, CIRCUIT, STICK, & LAYOUT OF SEVERAL INTERESTING SUBSYSTEMS.

(examples. on order of small to moderate first project)

[NO CLASS NEXT TUESDAY]

THURS (NEXT WEEK): { HOW ARE DESIGNS ARE IMPLEMENTED (INTRO)
HOW TO DESCRIBE LAYOUTS: USE OF SYMBOLIC LAYOUT LANGUAGE.

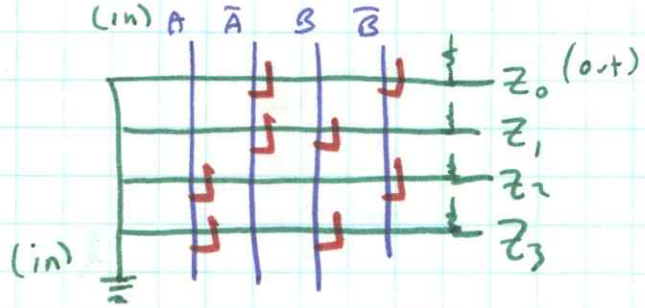
- HAND IN HW #3
- ILL HANDOUT HW #4 next time. I want to see how you did with these layout problems first --- PROBABLY WILL BE A STICK + LAYOUT OF ONE FET
- Start Thinking About projects. During next two weeks you'll finish all the basics you need to begin. Also we'll see more examples. Perhaps sketch out any ideas of interest. I urge you all to find collaborators: for at least design checking. Talk to others - it may help you get an idea - if you have more than one idea - share with others. I will hand out a questionnaire sometime soon to see how you are coming along on these preliminaries. Constraints, Alternatives, Post Mortems?

6.978. LECTURE #7 TUES OCT 3

- Discuss HW #2 before we begin lecture:

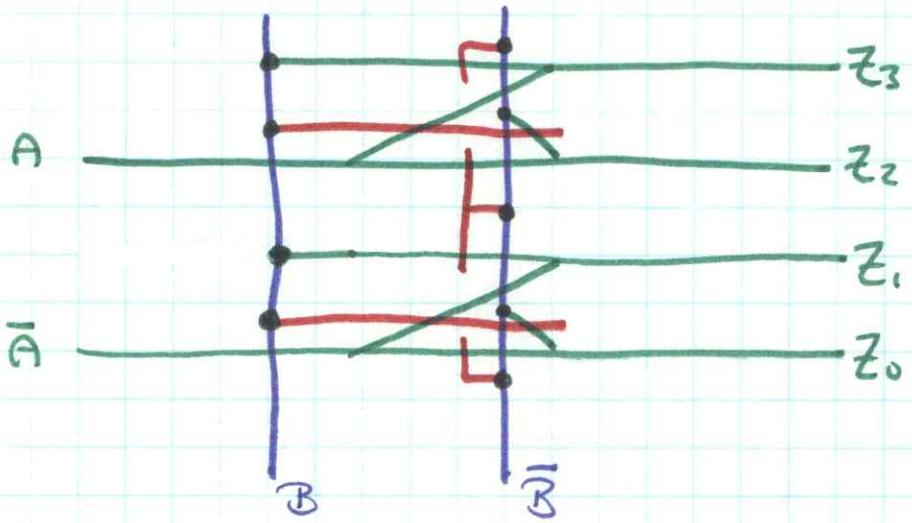
(PROB 5)

> As we'll see later, our old friend the "selector" circuit will turn up to have many uses when installed in different ways. A solution to 5(a) is to reverse the input/output, and hook up VDD & GND:



A B	z_0 z_1 z_2 z_3
0 0	0 1 1 1
0 1	1 0 1 1
1 0	1 1 0 1
1 1	1 1 1 0

> There are many other variants of this solution which are similar in structure. Ah! But look at the solution Clement Leung discovered using only a switch array with no VDD & GND:



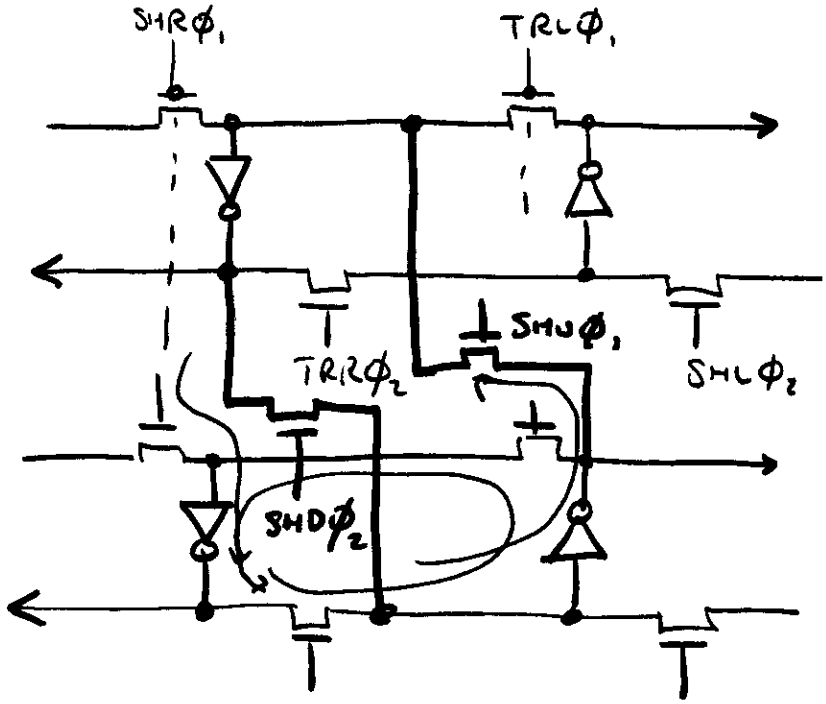
For example: If $\bar{A}=1$, then $\bar{B}=1$ passes to z_0, & $B=0$ blocks move up and more down, and $\bar{B}$ passes $B=0$ to z_1

If $\bar{A}=1$, then $B=1$ passes to z_1, $\bar{B}=0$ blocks more through, $\bar{B}=1$ passes $B=0$ to z_0

, etc.

HW #2 (cont.)

> **THE 2-D STACK:**
(Prob 6)



Some errors: running straight up/down, so signal propagates across array (data lost).

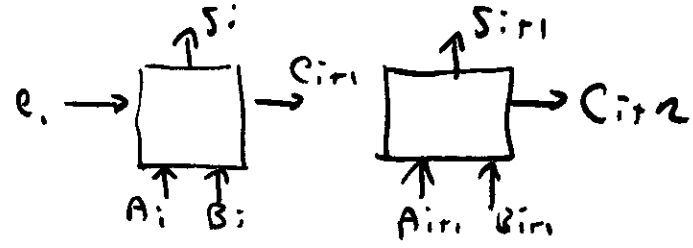
[Note that inverter output goes thru clocked line into node having no other inputs active, and outputs blocked by unclocked lines. For example, this doesn't happen →⊣]

Another error: Cycling SHU, SHD ended up shifting data right or left

> **MANY** (Stick) layouts possible. Don't know what might be best layout.

> **The Adder:** Most people got right answers for details of PLA's for problems 7 & 8.

However:



Draw Don't clock the carries

unless specify **CONTEXT** As Serial Adder

HW (cont.)

- I don't check all details of PLA code, just one or two product terms, ~ 1 output, & consistency. If you aren't sure of them, recheck them, & ask questions.
- Note importance of **context** of next level: does structure at one level not only satisfy the "rules" of that level, but fit properly at the next. Example: the "clocking of the adder."

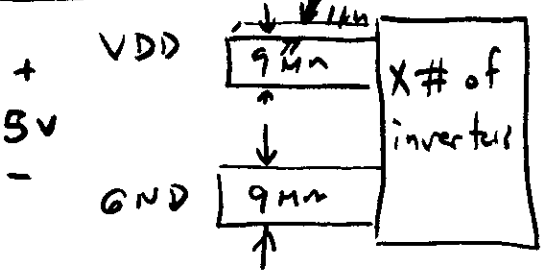
FROM LAST TIME: Rushed thru an important point. Repeat it too make sure you've noted it (Also, as you must now see - we want to get things right at the higher level before we start hacking out the layouts):

OM SLIDES

Question: How many minimum sized inverters will a minimum size VDD -- GND wire supply?

Line is $3\lambda = 9\mu m$ wide by $\sim 1\mu m$ thick:

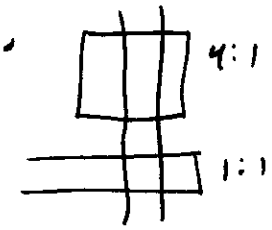
Have a bunch of inverters:



FOR 4:1 INVERTER,

$R \sim (4+1)10^4 = 5\times10^4\,\Omega$

$\therefore I = \frac{5}{5\times10^4} = 0.1\,mA$



> **LIMIT** $\tilde{=} 0.5\,ma/\mu m^2$, $\therefore$ 9μm wire carries ~ 5ma $\therefore$ **X ~ 50**

> But Half are usually off $\therefore$ X ~ 100

> And if 8:1's, then then X ~ 200

> But if mike 8:1's like 

then X ~ 100

BEGIN MAIN LECTURE:

AS WE'VE SEEN, CIRCUIT/SYSTEM CONSIDERATIONS OF POWER & DELAY AFFECT LAYOUT GEOMETRIES:

> WE ALMOST ALWAYS USE MIN L PULLDOWNS, FOR MIN T, BUT PULLUP LENGTH IS A FCN OF RATIO CONSIDERATIONS.

> WIDER PULLDOWNS (& PULLUPS) DRIVE LOADS FASTER, BUT ARE SLOWER TO BE DRIVEN.

YOU'VE SEEN HOW TEDIOUS LAYOUT IS (AND THERE IS STILL ONE MORE STEP IN INSTANTIATION: LAYOUT DESCRIPTION TO GO! ... WE GET TO THAT NXT WEEK).

> SO LET'S GO BACK AND MAKE SURE WE UNDERSTAND DELAYS IN DRIVING CAPACITIVE LOADS A BIT BETTER. ALSO, HOW TO MAKE BETTER DRIVERS. ETC

DRIVING LARGE CAPACITIVE LOADS:

SLIDE: Remember Fanout? The bigger the load, the slower it is driven.

Question: What do we do if we have a really BIG load? For example, going off-chip?

How can we drive a big C_L in minimum time, starting with signal on gate of MOSFET of C_g?

(1) Define $C_L/C_g = Y$.

Intuitively, we might think to drive a larger inverter from C_g, then a larger one, etc., until at some point we have an inverter big enough to drive C_L.

(2) Suppose we cascade inverters, each larger by a factor f.

Then each stage has a delay of fT (true to first order) we'll see why later

(3) If inverter delay is τ (or prop. to τ forgetting k for the moment) — will see why in Sinv Buffers

then **N such stages have a delay of $= Nf\tau$.**

(4) But $f^N = Y = \dfrac{C_L}{C_g}$

(5) If use large f, need fewer stages (smaller N) but each stage will have longer delay.

If use small f, need more stages, but each will have shorter delay.

Suppose $Y = 16$, could use $f = 2, N = 4$ or $f = 4, N = 2$

What N minimizes overall delay for given Y?

$$f^N = Y; \quad \ln(Y) = N \ln(f) \quad : \quad \therefore N = \ln Y / \ln f$$

Delay of one stage $= f\tau$

Total delay $= Nf\tau = \ln(Y)\left[\dfrac{f}{\ln(f)}\right]\tau$

$\therefore$ Delay is proportional to $\ln Y$

Figure 5 plots $\dfrac{f}{\ln(f)}$ as fcn of f, normalized to its minimum value of e

The minimum total delay = τ times e times natural ln C_L/C_g

$$\text{Min Tot. Del.} \sim \tau e \ln\left[\frac{C_L}{C_g}\right] \quad \text{when } f = e$$

O.K. What does this mean? The implications are really quite important:

> Off chip drivers go fastest when you build up with a factor of e per stage.

> But, speed isn't everything. If back off to $\tilde{f} = 6$, Almost as fast, but less area.

> SHOW ON DRIVER SLIDE

[Discuss the whole issue of the additional Benefit To be derived from VLSI: Less offchip Boundaries to cross.]

[Use of inword compatible Designs; Not optimized to current chip size, to develop scalable designs for VLSI]

There will be further important uses of this simple set of ideas in the development of a Theory of the space, time, and energy costs of computation in hierarchically organized systems, in Chapter 8 pp 49-57

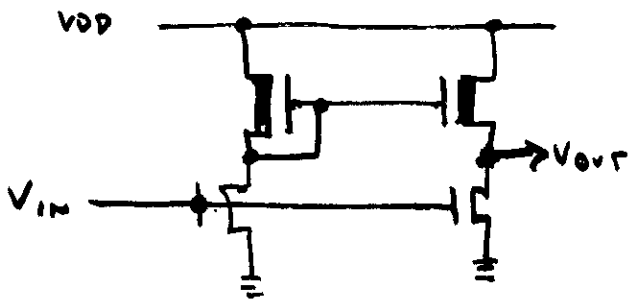
SUPER BUFFERS

- Ratio Logic as we've seen has an asymmetry:

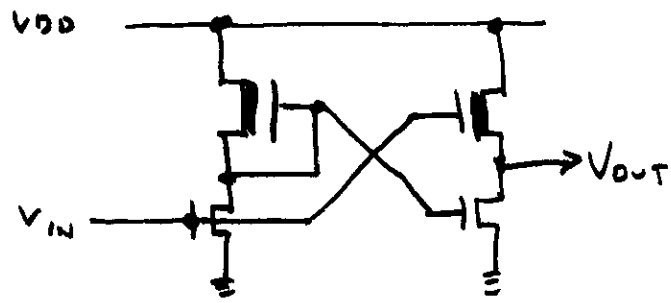
  It can discharge a C_L thru its pulldown much faster than it can charge one thru its pullup.

- There are ways of getting around this problem, esp. useful for drivers (at edges of arrays):

- Here are two circuits which are approximately symmetrical in their drive capability, even though they have 4:1 Z ratios:



INVERTING SUPER BUFFER



NON-INVERTING SUPER BUFFER

- IN EACH CASE, WHEN PULLDOWN INPUT TO 2ND STAGE IS ~VDD, THEN THE PULLUP GATE ~ 0V AS IN USUAL INVERTER. SO PULLDOWN THE SAME

- BUT, WHEN PULLDOWN INPUT TO 2ND STAGE GOES TO ZERO,

  THE PULLUP GATE GOES RAPIDLY TO VDD, SINCE IT IS ONLY LOAD ON PREVIOUS STAGE.

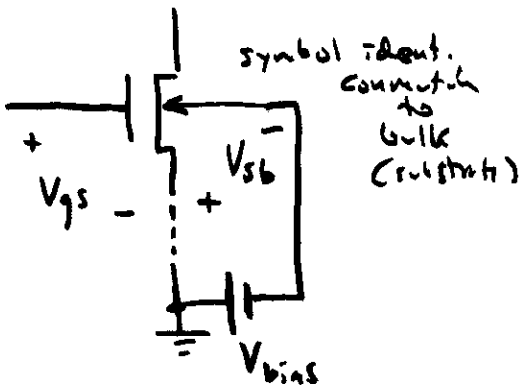
> The PULLUP is TURNED on with ~ 2x the voltage it would normally have with gate tied to source.
> Since in saturation, $I \propto V_{gs}^2$, the SUPER BUFFER PULLSUP about 4x as fast as regular inverter.
> i.e., PULLUP / PULLDOWN are ≈ symmetrical. $\frac{1}{4} = \tau$

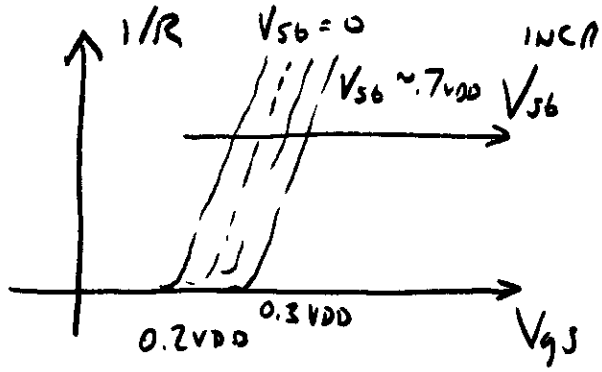
[that's why we got away with τ in the last section]

some eg. cases of using super buffer.

The Body Effect: We've considered V_{Th} to be a constant, independent of the source to substrate voltage (i.e., only a few of V_{gs}).

- It ain't quite that simple. Consider:





- So, V_{Th} gets larger as we raise the source voltage up from ground. Comment again on V_{gs}, V_{sb} ---

Why Is This Increase Important?

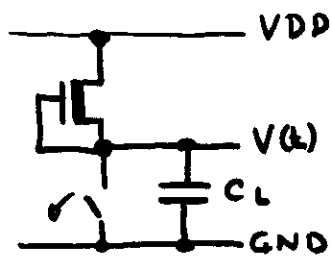
- Because it increases 2 effects we've already introduced informally:

  (1) The difference in time and final output voltage between an enh. & depl. mode FET driving a capacitive load.

  (2) The need to increase the Pullup / Pulldown Z ratio, when coupling logic stages by pass transistors.

DEPLETION MODE vs ENHANCEMENT MODE Pullups:

Depletion Mode (what we'll normally use):



- In the mid to latter stages of a rising transient, $V_{gs} \geq V_{th}$ and $V_{gd} \geq V_{th}$
- So the pullup is in its resistive region.
- The final stages of the rising transient are given simply by the exponential:

$$V(t) = VDD\left[1 - e^{-t/RC_L}\right]$$

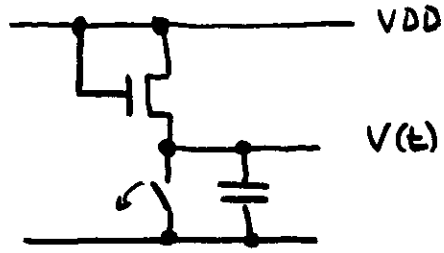
i.e., V(t) goes rapidly to VDD, with time constant RC_L.

- For inverter ratio k, pulldown tran time τ and gate C C_g, the time constant is

$$RC_L \sim k\tau C_L/C_g$$

Enhancement Mode

(used in early MOS)



- Since $V_{gd} = 0$, the pullup is in saturation whenever $V_{gs} > V_{th}$
- The problem: As the output voltage approaches $VDD - V_{th}$, the current supplied by the FET decreases rapidly
- In the Book, we derive: for large t:

$$V(t) \cong VDD - V_{th'} - \frac{C_L LD}{\mu\varepsilon Wt}$$

SHOW SLIDE AND COMMENT

[worsened by body effect]

Depl. mode crisply goes to VDD.
Enh. slowly (never) quite makes it to $VDD - V_{th'}$ (body effect)

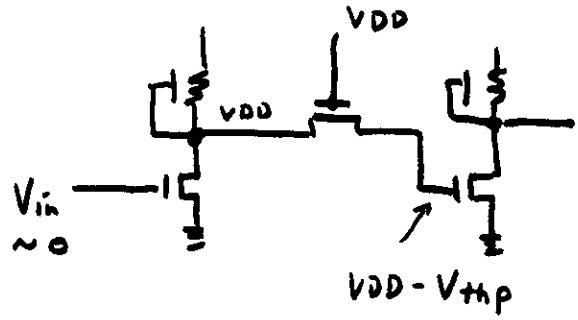
(IF TIME)

Pullup/Pulldown Ratios For Inverting Logic Coupled by Pass Transistors.

- We found earlier that $4:1 = Z_{pu}/Z_{pd} = \frac{L_{pu}/W_{pu}}{L_{pd}/W_{pd}}$

  yields equal inverter margins and also provides output sufficiently less than V_m for input = VDD.

- For stages of inverters coupled by pass transistors, such as



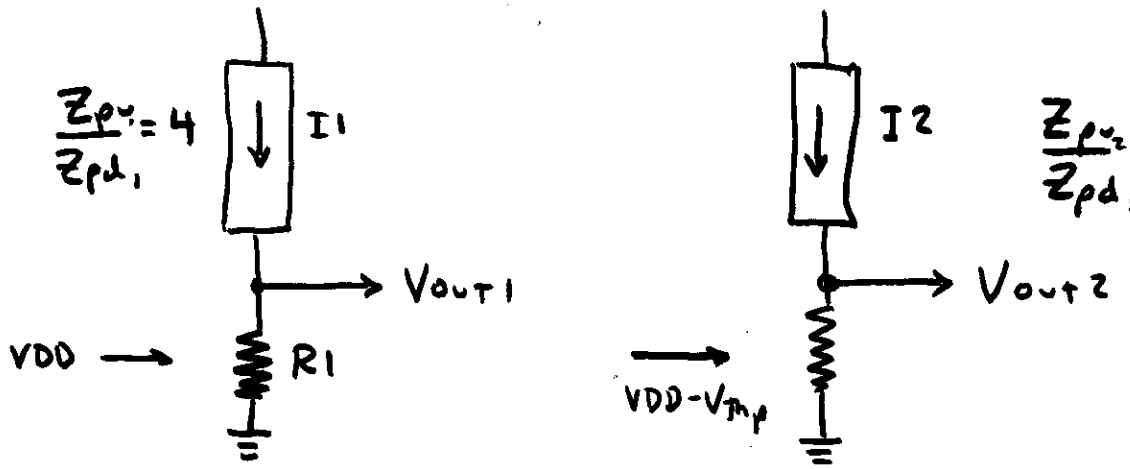
- If input to first is zero, and thus output ~VDD. If Pass T input is VDD, then at most the input to the second stage is $VDD - V_{thp}$.

- Since Pass T source is near VDD, V_{thp} is near its maximum of $\approx 0.3VDD$.

Question: What must be the Z_{pu}/Z_{pd} of second stage, if it is to have its output go as low with input = $VDD - V_{thp}$, as would a 4:1 with input VDD?

- With INPUT near VDD, the pullup is in saturation, and pulldown is in resistive region.

compare the two equivalent circuits:



- For V_{out1} to equal V_{out2}, $I_1 R_1$ must = $I_2 R_2$.
- IN SAT: $I_{ds} = \frac{\mu \varepsilon W}{2LD}(V_{gs} - V_{th})^2$ (eq 5)
- IN RES: $R = \frac{V_{ds}}{I_{ds}} = \frac{L^2}{\mu C_g (V_{gs} - V_{th})}$ (eq. 3a)

Substituting we will find:

$$\frac{Z_{pu_1}}{Z_{pd_1}}\left[VDD - V_{th}\right] = \frac{Z_{pu_2}}{Z_{pd_2}}\left[VDD - V_{th} - V_{thp}\right]$$

- Now: V_{th} of pull downs is $\approx 0.2\,VDD$, and V_{thp} of pass Ts is $\approx 0.3\,VDD$ to $0.35\,VDD$. (to be safe)

BODY EFFECT

$\therefore \; Z_{pu_2}/Z_{pd_2} \sim 2\, Z_{pu_1}/Z_{pd_1}$

$\frac{Z_{pu_2}}{Z_{pd_2}} \sim 8:1$

(WE USUALLY EITHER SPECIFY OR MEASURE ~~FOR INVERTERS NAND, ETC~~)

~~- WILL HAND OUT HOMEWORK NEXT TIME~~
~~- IF TIME, TALK~~

REMEMBER, THINK ABOUT PROJECTS A BIT.

[Think about what you'd like to do. Sketch out some ideas. Talk to others. Would you like to collaborate? On project? or just for checking? Any ideas others might use?]