LECTURE #3: 19 SEPT:

- Pass Out HW #2(a)
- Hand In HW #1
- How Many Think They found a reasonable solution to Prob. 2(a)?
- Are you interested in seeing a solution? Stick Diag. Dicks Soln. [Put on White Board ?]

Where we are:

Put on Board Before Class

This Week We Move Up a Level: • Discuss Inverter Delays, & A Clocking scheme. Then:

- We'll learn how to make Registers.
- We'll study an example subsystem: A Stack
- We'll learn how to impl. irreg C/L in a regular way using PLA's
- We'll learn how to implement Finite State Machines using registers & PLA's.

Next Week We Move down a Level:

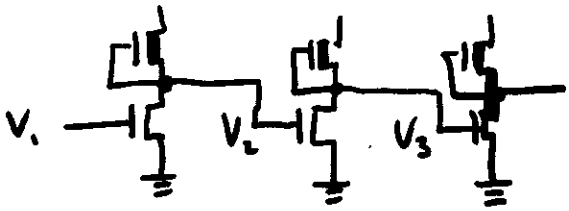
- Study the Silicon-gate nMOS process.
- Based on that, we'll develop a set of Design Rules which constrain how close we place wires, how narrow they may be, etc. (Geometrical Constraints)
- These Design Rules + rules based on the electrical properties of FET's and wires (such as the 4:1 rule) will determine how we may layout our stick diagrams.
- We'll Look at some example layouts

INVERTER DELAY:

[We'll come back to the topic of delay a number of times, treating it in more detail each time]

- Resistive Region: $\tau = L^2/\mu V_{ds}$
- Saturation Region: $\tau = L^2/\mu(V_{gs}-V_{th})$ { larger V_{ds} doesn't reduce τ

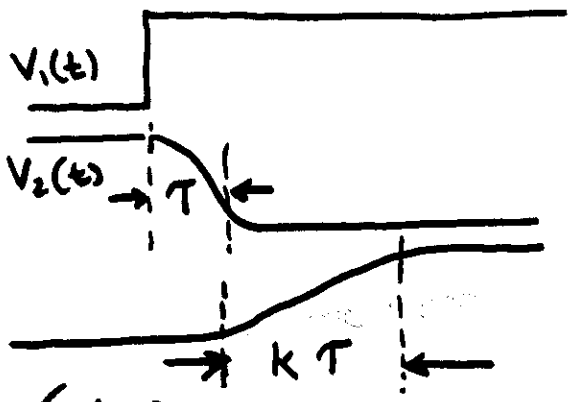
- Examine case where an inverter drives succeeding similar inverters:



Suppose: $V_1 = 0$. Then at $t = 0$,
Drive $V_1 \rightarrow VDD$.

What happens?

Graph of Effect:



- It takes ~ τ (mean) to remove the "positive charge" from the C_g of the second stage - thru the pulldown of the identical first stage.
- When second stage turns off, 3rd stage C_g charges up (thru pullup of 2nd) to VDD.

(τ of Pullup ~ 4 x τ of Pulldown)

- But pullup has less current capacity than pulldown, so this charging up takes longer, by ~ ratio $k = \tau_{pu}/\tau_{pd}$.
- So normally speak of inverter pair delay $= (1+k)\tau$
- If Fanout f (i.e. 1st feeds f next stages in //) or if next C_g is larger by factor f, then multiply switching delay time by factor f.

Some Approx Values in 1978

- Small FET's have gates $6 \times 6\ \mu m$
- Resistances

  Metal $\sim 0.1\ \Omega/\square$, Poly $\sim 15\text{-}100\ \Omega/\square$, Diff $\sim 10\ \Omega/\square$

  Transistors: $10^4\ \Omega/\square$ Note: Res FET's >> Res wires
- Capacitances: (to substrate)

  Metal $0.3 \times 10^{-4}\ pf/\mu m^2$, Poly $\sim 0.4 \times 10^{-4}$, Diff $\sim 0.8 \times 10^{-4}$

  Transistor Gates: $\sim 4 \times 10^{-4}\ pf/\mu m^2$

  Note: C_g only X10 that of wires. But wires typically X10 area of gate they feed. So typically must multiply X2 the gate capacitance to estimate delays. (Call this parasitic capacitance)
- Calculate τ Two ways: (Ballpark, to get order of magnitude)

> $\tau \approx L^2 / \mu \left(\frac{VDD}{2}\right)$ Now good, $\mu = 800\ cm^2/volt\text{-}sec$

$\tau \approx (6 \times 10^{-4})^2 / 800\left(\frac{5}{2}\right) \cong .18 \times 10^{-9} = 0.18\ ns.$

So actual inverter τ (incl. x2 for parasitics) = **0.36 ns**

> $\tau \approx R_{FET} C_g \times 2_{PARASITICS}$

$\tau \approx 10^4 \times 4 \times 10^{-4} \times 10^{-12} \times 2 \times 36_{(nm^2)}$

$\tau \approx 288 \times 10^{-12} \cong$ **0.29 ns**

- Above are actually what we would measure for τ in Ring oscillators for the best current 6 μm processes. Over many processes, typically $0.3 < \tau < 1.0$ ns

NOTATION: You've read about Notation. In partic, **MIXED NOTATION** While not formalized, yet will be very useful. Will become clear by example. Useful to

> Reduce clutter in diagrams. Parts of less detailed interest can be left in higher level form.
> Diagram designs when only some of the details have been derived and/or bound.

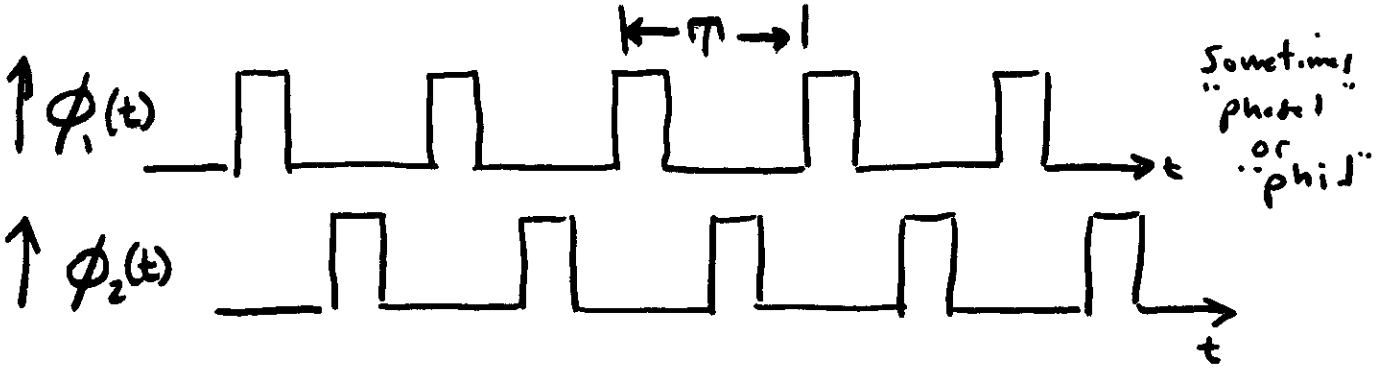
>>> SOMEDAY I easier to visualize FSM with a particular type of mixed notation

TWO PHASE CLOCKS: (START OVER ON BB)

We will use one particular clocking scheme to determine times when we'll allow data to enter and update the contents of registers in our systems:

We call it: **Two-Phase, Non-Overlapping clocks**

Let's **PLOT THE CLOCK SIGNALS AS FCN(t):**



> The signals switch between ~0 volts and ~VDD.
> Both have the same period T.
> The high times of both are shorter than their low times
> They are never both high at the same time, i.e. they never overlap.

[What the lock masters must never-never do > open]

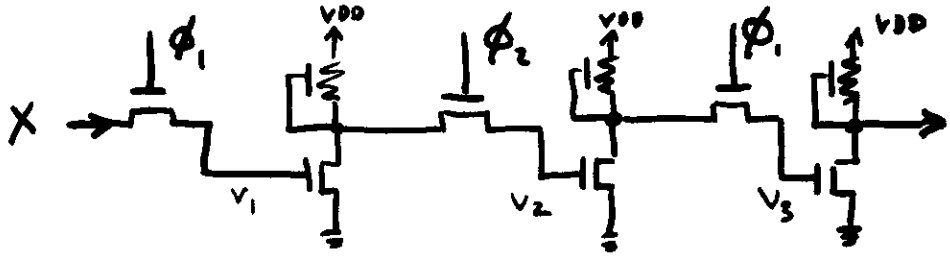
- **TIMING/SYNCHRONIZATION** are in the general case subtle, complex. We'll come back to this later. For the sort of systems... synch-dig. the 2-ϕ is perfectly O.K.

THE SHIFT REGISTER:

- Perhaps the most basic structure for moving a sequence of data bits. It is the basic structure from which we will derive our notion of "Registers" and R-R Transfer

- Draw circuit diagram:

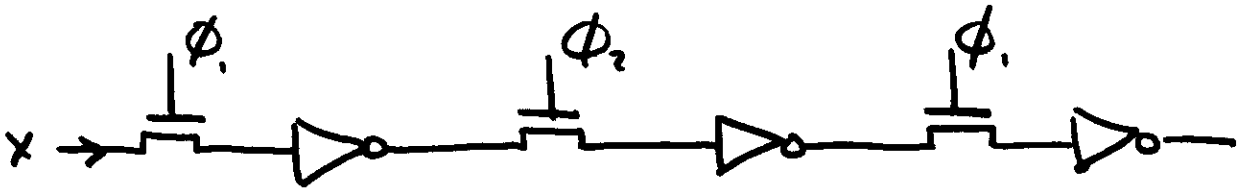
maybe graph V_1, V_2, V_3 vs ϕ_1 ϕ_2



- Describe movement of data during ϕ_1 followed by ϕ_2

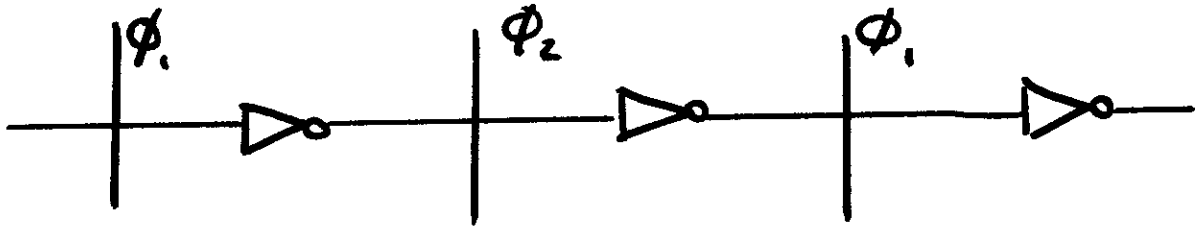
(mention term "pass transistor" or "transmission gate".)
as these transistor "switches" not part of pullup/pulldown static logic. i.e. They lead to capacitive loads only, NOT VDD or GND

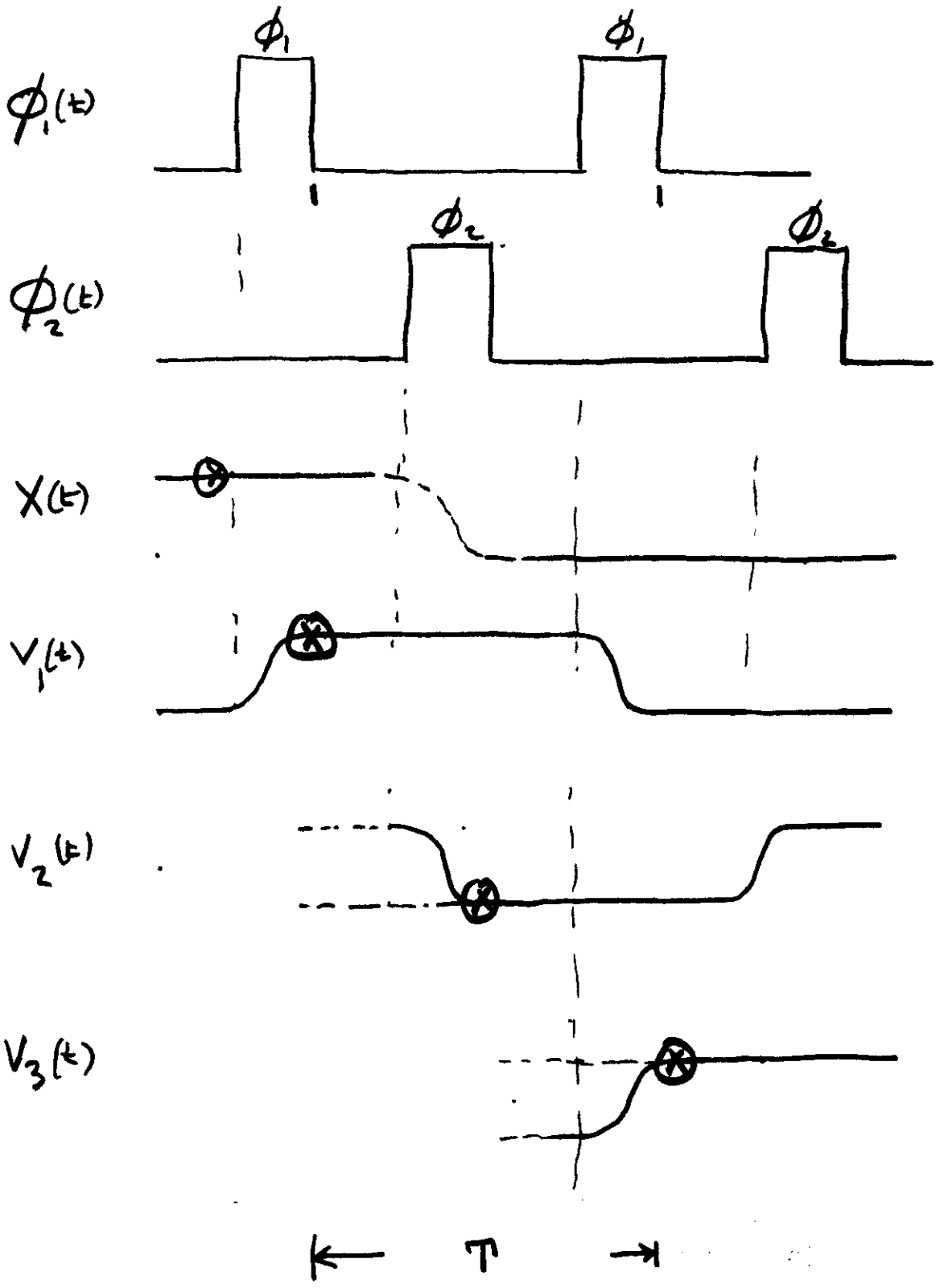
- Now show alternative diagram: mixed notation:



- Describe: especially: must envision the input of the inverter as leading to C_g, the gate of a FET.

- Now start to show part of stick diagram:



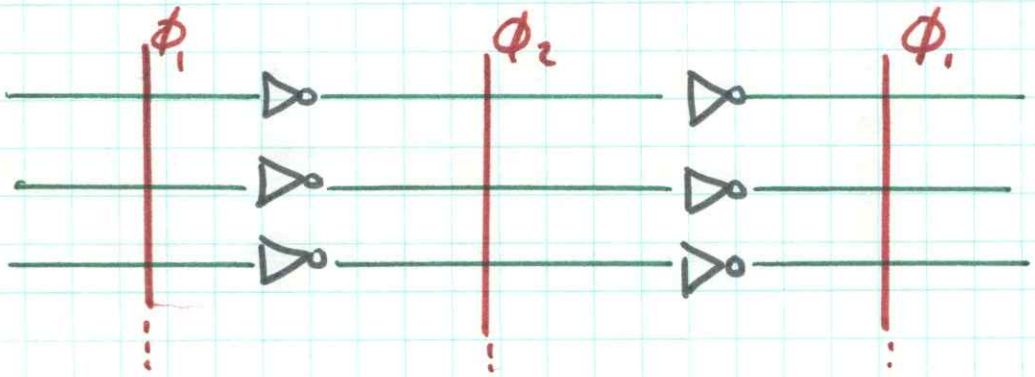


$V_1 \rightarrow V_3$ in $T = "\phi_1" + "\phi_2"$

Continue to Build on Shift Register Idea:

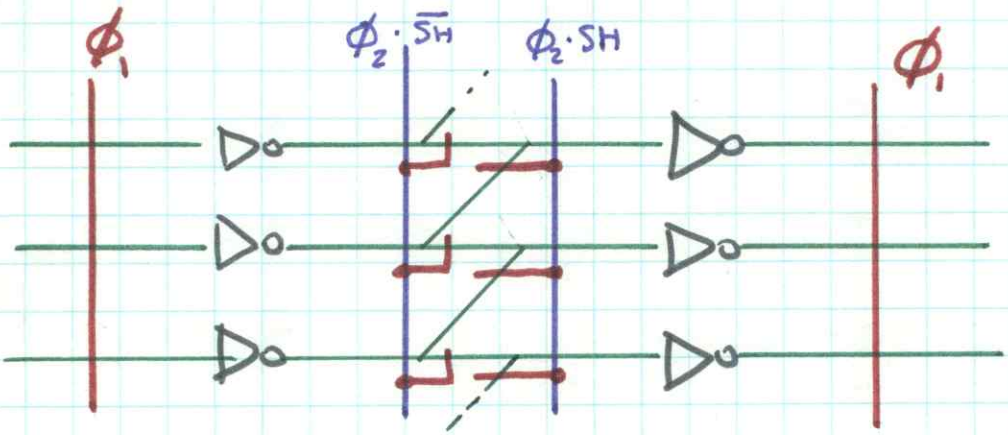
How could we move a sequence of words from register stage to register stage - rather than just a sequence of bits?

- By stacking together several shift registers in parallel, as follows:



- But this is just moving data around. How do we control the data movement: Ah: by putting some switching or C/L function in between register stages:

An example: Shift up / straight thru register stage:



(FLIP OVER TO VG SCREEN)

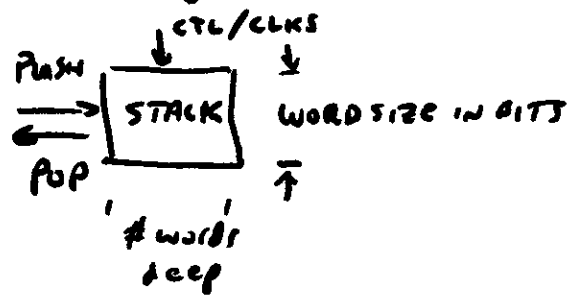
- DIFF LVLS OF ABSTR. SIMULTANEOUSLY PRESENT. HOW TO VISUALIZE FCN OF SUCCESSIVE INV LOGIC STAGES SEP. BY PASS TRANSISTORS?

  SHOW & DISCUSS FIG 6 SLIDE

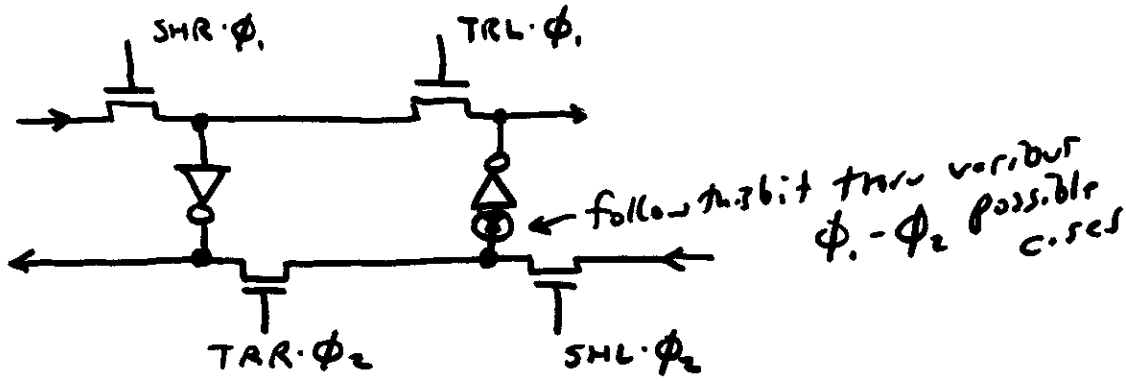
- HOW TO IMPL SIMPLE REGISTERS:

  SHOW & DISCUSS FIG 7-9 SLIDE

- DESIGN OF A STACK SUBSYSTEM (INTRO: TO BE CONT. NXTIME)
- TALK THRU BASIC IDEA:



- First Conceive of a cell design for one bit of one track:



- SHOW SLIDE AND DISCUSS LAYOUT (OR SKETCH)

- SHOW CONTROLLER CHIP SLIDE.

  (WELL SEE HOW TO COMPLETE THE OVERALL SUBSYSTEM DESIGN NEXT TIME, INCL. GEN. THE CTL SIGNALS)