6.978 LECTURE #16. NOVEMBER 14.

TODAY: MORE ABOUT THE FUTURE: HOW THE PATT'S FAB TECHNOLOGIES MAY BE IMPROVED TO ACHIEVE SCALING TO LIM. DIM.

FIRST: PROJECTS: NOTE: NO OFF. HRS. TMRW. FRIDAY INSTEAD

- Prof. Antoniadis is looking for several students to collaborate on designing & laying out electrical test patterns. These will be acceptable projects and any who haven't started work on a project yet - I suggest you speak with Prof. Antoniadis right after class. DIMITRI - perhaps you could say a bit more about this: ---

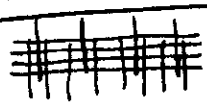
- There are some students who haven't yet turned in enough of the project assignments for me to get a clear idea of your project selection. Please see me after class if you are on this list. (I'll finish a bit early):
  Rae McClellan, Dave Levitt, Dave Shaver, Scott Westbrook, Moshe Bain, Martin Freeman.
  (FIFO) (multi-function memory) (test patterns) (clock generator)

- You may have noticed the OVG cuts in the PAD cells over the contact pads. We will be producing an OVG mask, which could be used in later processing to pattern protective OVG. However, in the fab of the project set, no OVG will be placed. You will therefore (may) be able to probe any large (> 25μm x 25μm) metal features as test points. Sometimes people put these in as contingencies (rather than bringing out all test points to contact pads.) But be careful of long C's AND gates can't be tested!

- A word about Functional testing: Testing uncovered chips requires reduced light levels. The operation of dynamic circuits using pass transistor input to a gate can be severely affected by light. Light induces leakage currents in the n-p junctions between source and drain and substrate. At room T, charge may be stored for a number of milliseconds on dyn. nodes IN ABSENCE OF LIGHT. However, in normal room light, this time may be reduced to tens of microseconds. Avoid light when long clock periods are used. Dyn. Mem. Chips packaged in Blk Opaque Packages because of this effect.

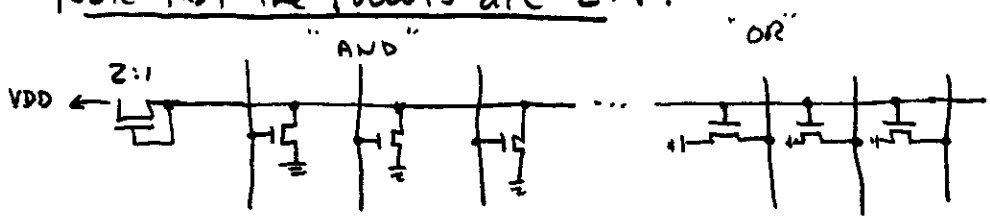
- ~2 weeks to get to prelim layout of entire subsystem. I want them to check IF want to get on fast chip out.

- **COMMENT ON WIRING STRATEGIES**



- **The PLA Library cells**: Several of you are using the PLA cells in your projects. You've already noted there are differences in the PULLUPS & the IN & OUT registers. The other cells look the same as those in the book. BUT, there is a key difference - I want to thank Glen Mitsubori for bringing this to my attention:

Note that the PULLUPS are 2:1.



It was designed so that the PULLDOWNS could be 1:2. This make the ratio 4:1 as required. BUT NOTE, if you programmed it with min width diffusion lines, you would make pulldowns that were 1:1, and overall ratio would be only 2:1.

Reason for 1:2 PullDowns: In large PLA, the limiting factor will or might be the FANOUT into the OR plane. The larger pulldowns and shorter pullups can source or sink more current and can thus drive this larger capacitive load twice as fast as the design in the book.

The 1:2 PullDown doesn't enlarge the basic PLA cell pitch area. We use a 4λ x 4λ DIFF box to place a transistor rather than a 2λ x 4λ box. Sketch on SLIDE

- **FINAL**: I had originally planned to give a Take Home Final Exam. However, I now think that such a final would be anticlimactic after the projects. I'd much rather that you put your energies into your projects and not worry about a final. So I don't plan to give a final.

Those who didn't do well on the midterm: please remember that I will be giving the PROJECT much more weight than the M.I.T. Exam. If you are still concerned — see me.

PATTERNING & FABRICATION IN THE FUTURE:

IN the previous lectures, we examined the quantitative effects on performance of scaling down the dimensions of devices in our systems, i.e. The effect of making things smaller. We also studied factors which limited such scaling ie. HOW small the transistor can be made and still function.

Now: How in fact can We make things That small? Recall that the limiting feature sizes were on the order of 1/4 micron feature sizes. The wavelength of visible light is ~ 0.4 to 0.7 μm. UV is ≈ 0.2 to 0.3 μm

- LETS EXPAND OUR VIEW OF THE FUTURE FROM THE SIMPLE TABLE GIVEN LAST TIME OF SIZE/PERF. as fcn time. TO INCLUDE HOW THESE CHANGES CAN BE BROUGHT ABOUT. NOTE: ALTHOUGH AS SYSTEM DESIGNERS WE WON'T NEC. BE INVOLVED IN THESE PATT/FAB TECH. CHANGES, WE MAY NEED TO KNOW ABOUT THEM, TO UNDERSTAND HOW THEY MAY AFFECT SYSTEM DESIGNS OR DESIGN FILE PREPARATION. THIS IS ESP. TRUE FOR THOSE COORDINATING PROJECT SETS.

- FOR THE DESIGNER WHO DOESN'T GET INVOLVED IN IMPL., OUR FILM PROCESSING ANALOGY WILL HOLD, EVEN THOUGH THE PROCESSING TECHNOLOGIES ARE RAP. CHANGING: WE'LL KEEP GETTING FASTER & FINER GRAIN FILM EACH YEAR - - -

AS WE PROCEED FROM 6μm to 0.3μm Feature sizes,

1. CIRCUIT & DEVICE TECHNOLOGY & DESIGN RULES & CONSTRAINTS
2. PROCESSING TECHNOLOGIES
3. PATTERNING TECHNOLOGIES

} WILL ALL BE CHANGING.

LETS EXAMINE THESE IN ORDER:

DESIGN:

(1) nMOS will very likely be a standard technology for high density/high performance LSI/VLSI for the next 4 to 6 years at least. When feature sizes go under 1μm, we will be forced into new device, circuit, system design techniques because of getting boxed into the current density vs power density corner as we saw last time. A likely candidate for the 1μm to 0.3 μm scaling is CMOS, which is similar as a medium for design.

However, we needn't be too worried about these changes. During the next 4-6 years, computer aids for design will be rapidly improved. Design will be done at a higher level - more like arranging the floor plans of subsystems and compiling stick diagrammed cell arrays from libraries into target design rules - with aids helping check for current/power density limits, etc.

So, as fast as changes in the way we design or constraints on design occur, we will get improved design aids - design should get much easier.

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(2) PROCESSING TECHNOLOGIES: Even if we could pattern resist with features smaller than the wavelength of light, current processes couldn't "develop the film":

Independent of any particular technology,
(a) diffusions produced by placing wafers in gases at high temperature, and (b) wet etching techniques, are not sufficiently controllable to achieve fine feature sizes.

Some solutions:

(a) Ion implantation is even now replacing earlier techniques for diff. of impurities into the substrate. Offers high degree of control over dosages, and high uniformity.

Basically, the wafer with patterned resist is simply exposed to ions accelerated in a big ion accelerator. The ion implanters are expensive, but in principle are simple. Also, easily automated. Wafers can be delivered on a truck and flipped into position in a lock, then exposed, then continue on.

(b) Wet etching gradually replaced by etching with Plasmas: i.e. by using glow discharges of gases to produce Free ions of great chemical activity. Again, here, can achieve great control over the etching process.

(c) How might we achieve high aspect ratio wires? Techniques are evolving. One possibility is called ion milling. Ions accelerated to modest energies sputter away metal not covered with resist. Can yield sides much steeper than with wet etching.

PATTERNING: O.K., maybe improved design systems will help us cope with changing technology & more design constraints, and process technology may evolve to etch or implant fine details. But how do we pattern resist with features finer than wavelength of UV light?

Patterning Technology is undergoing a rapid evolution. It is important that we have a feeling for this because a lot of information handling is involved in patterning & patterning technology imposes many constraints on designs and design files.

Also, great reductions in impl. turnaround time can be made by system designers working to take advantage of new patterning technologies — which provide opportunities for more automation of the overall process.

- LETS SKETCH THE COMING EVOLUTION IN PAT TECH BY BEGINNING WITH WHATS HAPPENING RIGHT NOW --- THEN WORKING FROM THERE.

(SLIDES) MOST FAB LINES USE "WORKING PLATES" TO MAKE A SORT OF "CONTACT PRINT" EXPOSURE TO PATTERN RESIST. THE PLATES GET DIRTY & WEAR OUT.

- SO: TREND IS TO PROJECTION EXPOSURE OF 2X (or higher) MASK ONTO THE WAFER. MASTER MASKS CAN BE USED (DON'T WEAR OUT). LARGER FEATURE SIZE ON MASK MAKES IT A BIT EASIER TO PRODUCE MASKS OF A GIVEN ON-CHIP FEATURE SIZE.

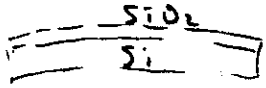
SUCH PROJECTION EXPOSURE WILL BE GOOD DOWN TO ½ μm FEATURE SIZES. BELOW THAT WE'LL NEED AN ALT TO UV light. BUT MORE THAN feat size to worry about. λ also result of ~1 μm

- BUT EVEN AT ≈ 2 μm Feature size ($\lambda = 1$ μm) WE

ENCOUNTER A PROBLEM WITH RUNOUT: So far we've always thought of exposing whole wafer at once. Can we continue to do this? Possibly not. Consider:

When bare wafer is heated, it expands. Now suppose SiO_2 is grown. Thermal coeff of exp of SiO_2 is ≈ 1/10 that of Si:

As wafer cools, Si shrinks more than SiO_2. So, wafer won't be flat, but will be convex on the SiO_2 side



Now if cooled slowly, may be possible to relieve the stress induced by the diff in ~~exp~~ contraction.

- But — while wafers might then be flat — they are of a slightly different size than originally. Unfortunately this change is pattern dependent, and so we can't resort to simply making successive mask layers larger.

- As wafers get larger, and feature size, smaller, at some point full wafer exposure must be abandoned because won't be able to align a successive layer over whole chip.

Alternatives to Full Wafer Exposure:

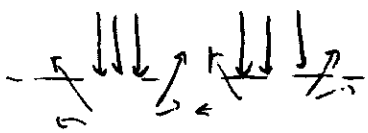
(i) Direct exposure of resist on wafer using an Electron Beam. The beam can not only expose, but can using a variety of techniques, sense a pattern previously produced, thus doing local alignment corrections.

(ii) Exposure using masks, probably projection of mask, but of less than full wafer. Step & Repeat with local alignment on the wafer to cover entire wafer.

When $\lambda < 0.5\mu m$, Feature Size $< 1.0\mu m$, we no longer can use UV light (wavelength $\geq 0.3\mu m$), since can't resolve features.

- What are the alternatives available? First, we could use an electron beam. Electrons accelerated to moderate energies will expose various resists. We can produce very narrow E-beams ~~< 250 Å~~, but there are problems which will likely limit use of Direct writing with E-Beams to feature sizes $> \sim 0.5\mu m$. Problems:

  > Main problem is scattering of electrons in resist and silicon. The exposure latitude narrows as the spatial period of a pattern is reduced:

  SHOW SLIDE OF CALC EXP.

  USING AS 250Å, 10KeV, resist 0.4μm.
  AT SPACINGS OF 2μm, 1μm, 0.5μm, 0.3μm.

  > Associated Problem: Exposure at any point depends on exp. at neighboring points. This proximity effect requires pattern dependent exposure corrections at small values of λ.

  > As λ decreases, the time to "write" the whole wafer rapidly increases. Time (expense) per wafer gets very large at small λ.

- However, although time/wafer may be long, the direct writing E-beam exposure offers possibility of shorter turnaround than when using masks. No masks to pattern and develop. The E-beam machine can be viewed as a COMPUTER OUTPUT DEVICE. We could have a different chip design in every chip position. IDEAL FOR MULTI-PROJ. CHIP SET IMPLEMENTATION. Especially if integrated into a relatively automated fabrication facility.

- O.K. But how do we do better than ≈ 0.5 μm, and how do we get high wafer throughput in manufacturing at < 0.5 μm feature sizes?

- ONE POSSIBILITY IS TO USE X-RAYS TO EXPOSE THE RESIST.
(MUCH OF THE PROGRESS IN THIS AREA IS RESULT OF WORK BY HANK SMITH AND HIS COLLEAGUES AT MIT LINCOLN LABS.)

WE GET AROUND THE WAVE LENGTH PROBLEM BY USING SOFT X-RAY RATHER THAN UV. TECHNIQUES FOR OPTICAL ALIGNMENT (INTERFEROMETRIC TECHNIQUES) ARE NOW KNOWN WHICH CAN ALIGN TO ≈ 0.02 μm.
XRAYS OF ≈ 100 to 1000 eV range (WAVELengths ≈ 0.01 to 0.001 nm)
SO, WE CAN USE THE STEP & ALIGN TECHNIQUE TO ULTIMATELY SMALL DIMENSIONS USING ORTICAL INTERFEROMETRIC ALIGNMENT AND X-RAY EXPOSURE.

- WE ARE THUS BACK TO MAKING MASKS:

OK on next pg

X-RAYS REQ. A VERY THIN MASK SUPPORT: e.g. MYLAR, UPON WHICH A HEAVY METAL SUCH AS GOLD OR TUNGSTEN IS USED AS THE OPAQUE MATERIAL.

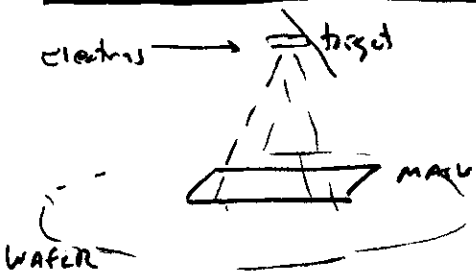
NO BACKSCATTERING OF XRAYS OCCURS. INTERACTIONS OF X-RAYS WITH MATTER TEND TO BE ISOLATED, LOCAL EVENTS. ANY ELECTRONS PRODUCED WHEN XRAY ABSORBED ARE LOW ENOUGH IN ENERGY SO RANGE IS ONLY SMALL FRACTION OF MM.

- SO, PATTERNS PRODUCED BY X-RAYS IN RESIST ON SILICON ARE MUCH CLEANER & BETTER DEFINED THAN THOSE PRODUCED BY ANY OTHER KNOWN TECHNIQUE (SLIDE) SLIDE SHOWS PAD WITH PERIOD OF ≈ 0.3 μm.

- HOW DO WE MAKE THE X-RAY MASKS?

  ANS: USING AN E-BEAM MACHINE!
  (O.K. IF IT TAKES A WHILE TO EXPOSE, SINCE WILL USE MANY TIMES)

- A Problem with X-RAYS:



If use traditional method of producing soft x-rays, have problem of not a "point source" and beam is not collimated. So, if get close to source to get higher intensity, feature resolution is poor. If far away, Exposure times too long.

- A solution: Use a Storage ring (synchrotron) to produce the X-rays. A 500 to 700 MeV electron storage ring shaped as a many sided polygon. Beam deflected at each "corner" using superconducting magnets. Deflection results in a centripetal acceleration of electron and hence in intense tangential emission of synchrotron radiation. The most important component of such radiation is soft X-rays. Could fit one exposure station to each vertex.

  Alignment would be done by an automated optical interferometric technique, on a per chip basis.

  X-ray intensity in such a system is high enough that one layer of our chip could be exposed at each vertex every few seconds. Achievable values of λ in both the feature size and alignment sense are down to $\lambda \approx 0.1\,\mu m$.

- AN OVERVIEW OF POSSIBLE FUTURE ROUTES FROM DESIGN FILES TO FINISHED CHIPS WITH MICRON TO SUB-MICRON FEATURES IS GIVEN IN FIG 27 (SLIDE)

- IN IMMED FUTURE: MANUF OVER NEXT 3-4 YRS:

  PROJ. EXP. WILL WORK DOWN TO ≈ 1-2 μm feature size AND PROJ. EXP + STEP & ALIGN ON WAFER WILL GET AROUND ANY RUNOUT PROBLEMS.

  . THIS ALSO ELIMINATES STEP & REP. IN MASKMAKING. COULD HAVE REASONABLE TURNAROUND IF OPTIMIZED FOR THAT (TREND TO MAKING OPT MASKS BY E-BEAM: SIMPLER, QUICKER, THAN P.G.)

- RIGHTMOST PATH: DIRECT WRITING WITH E-BEAMS:

  WHILE SLOW/WAFER PATTERNED, NEVERTHELESS PROMISES THE ULTIMATE IN SHORT TURNAROUND. A LIGHTLY LOADED HIGHLY AUTOMATED PROTOTYPING FACILITY WOULD BE ULTIMATE FOR QUICK DESIGN DEVELOPMENT. WORKABLE DOWN TO $\lambda \approx 0.3\,\mu m$ Features 0.5 to 0.6 μm

- CENTER PATH: POSSIBLY THE ULTIMATE MANUFACTURING

  PATH FOR DENSEST SYSTEMS. CLEARLY WORKABLE FROM PATTERN FEATURE SIZE & ALIGNMENT STANDPOINT DOWN TO $\lambda \approx 0.1$ μm. (Feature 0.2 μm) i.e. to limiting dimensions.

[NOTE: Process Tech.; Device Circuit & System Design Methodology must evolve with all this.]

- Could imagine: Prototyping Design in Q.T. environment at $\lambda = 0.5\,\mu m$, then manufacturing full systems at $\lambda = 0.2\,\mu m$.