6.978. LECTURE # 12. 24 OCTOBER '78

- Handouts: HW, CIF Tran Guide, Guide to LSI Implementation
- Announce: Lab is running. Software & Plotters working.
  2 Lab assistants: Charlie Davis, Philip Ngai.
  Rm 36-561. Open ~3 to ~8+, Mon-Fri.
  PROJECT IDEAS
- TODAY: Design & Implementation: More on how actually done at present. How we'll do it. Details that aren't in Text.
- Impl. Guide cont. much of this mat'l. Background: Was prep. for instr., TA's, Lab Assistants, for courses starting this year ---. But there is a lot of gen. useful info, so I had copies made for all of you. ---
- So, today we'll skim thru a wide range of practical topics to get feeling for how things are really done now. Mostly we'll skim thru the Impl. Guidebook.
- Some of this will be useful reference mat'l for projects
  [For example, there is a cell library in CIF in GuideBook]
- All of this will set stage for looking ahead into the future: What would we do differently? ---
- In Later Lectures: We'll study future patt/fab techniques which'll enable higher density, & the effects of this ---

BUT THERE IS MORE TO THE COMING CHANGE: We'll consider at least 3 areas:

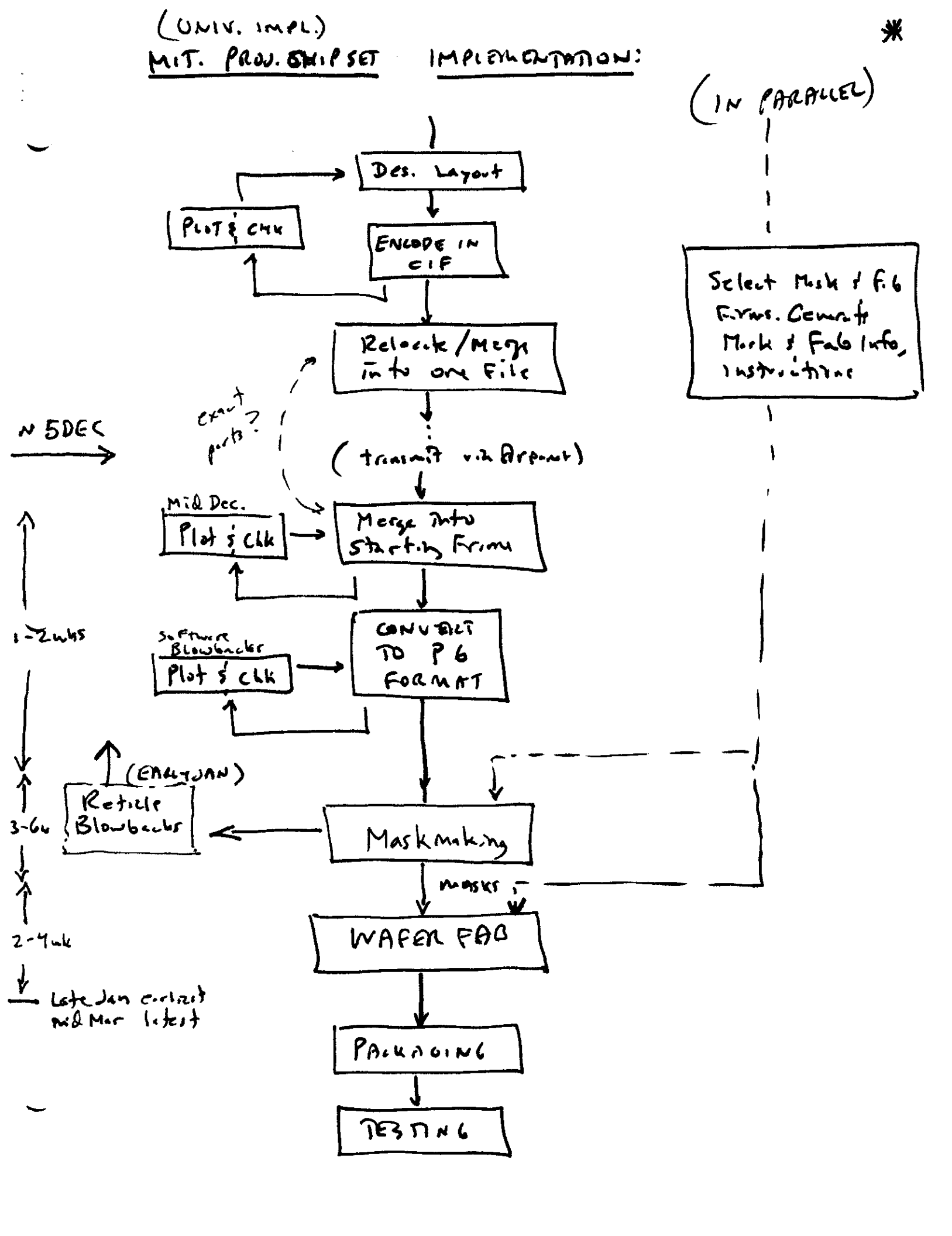
1. IMP. DES AIDS: FASTER/EASIER DESIGN
2. MORE PROC. AUTO: FASTER IMPLEMENTATION
3. HIGHER DENS.: SCALING EFFECTS

- OVERVIEW/REVIEW OF DES & IMP (SLIDES)
  "ARTIFACT FLOW"
- NOW, HOW ARE WE ACTUALLY GOING TO DO ALL THIS?
- DRAW FLOWCHART ON BOARD *

MANY OF THE ANSWERS, IN DETAIL, ARE IN THE GUIDEBOOK.

(UNIV. IMPL.)

MIT. PROJ. CHIPSET IMPLEMENTATION:



- I'd like to go thru the Guidebook in "LOGICAL ORDER"

  Skimming some sections, just indicating contents, Going into more detail on other sections.

  All this is to raise your awareness about the range of topics. You'll know where to look to begin to get answers. Also recommend the Sep'77 SCI AM issue for more "LORE". But it and most other ref. are written to describe what "Someone else" does rther than teach you how to do it.

- TOPICS IN LOGICAL ORDER:
  - > DESIGN AIDS: BASIC IDEAS, PRAC THINGS YOU MIGHT USE.
  - > PRESENT MASK & FAB PROCEDURES
  - > MULTI-PROJECT CHIP & STARTING FRAME
  - > INTERFACING MASK & FAB FIRMS
  - > WHEN WAFERS COME BACK: PACKAGING
  - > TESTING: ELECTRICAL, FUNCTIONAL

- DESIGN AIDS: SKIM THRU, IDENTIFY A FEW SECTIONS:

- INTRO SECT (P 5-8) S.TRIM., "AUTOMATED DESIGN AIDS"
  - > Desc. Basic Des.Sys (CIF → Plotter as here)
  - > Symb. Layout > Inter. Graphics
  - > Ideas regarding Future ADV. Des. Systems

- More Detail on Symbolic Layout: (p 9-15) M. Stone. Discussion of what symb. layout languages might do. Later, a SPEC of a proposed language (ICLIC) is included (p. 79-99)

- Design Rule Checking: Short but interesting discussion (p 15-18) by w. wilner. Not trivial problem. Industrial programs exist purporting to "check design rules". Note that till now no formal description of any design rules has existed. ALL AD HOC

  We will include in publ. text a recently completed formal desc. by Irene Buchanan of Edinburgh of our design rules.

In long run: Prob best to Inst. Layout from sticks as few rules, R.T. CHEN

One Design Aid You'll Find Useful: A Cell Library

(p 100-144) Bob Baldwin, Dick Lyon

- A bit about managing a Cell Library. 100-101
- Table of Contents 102-103

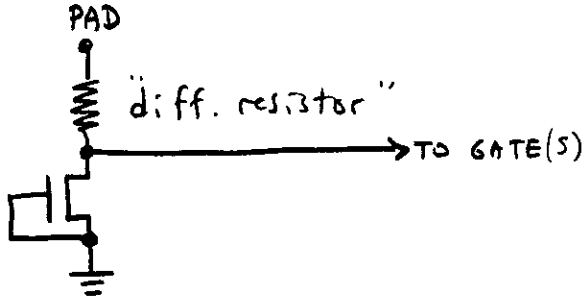
- **SOME USEFUL CELLS:** Pads, PLA cells, Logic/Arithmetic, & STARTING FRAME (disc. later)

- **PADS:** Input w lightning Arrestor, Output with Driver, VDD, GND, Blank. p 104-111. SLIDES

Cleverly Designed so they all fit together on same pitch. VDD runs along top & sides. GND along bottom.

EXAMPLE: **PADIN:**

Normally, FET is OFF, so circuit behaves as resistor connected to pad.



But, if Voltage becomes large (i.e. Pad struck by lightning) then FET will punch trough, current will Flow dropping the over voltage across the resistor.

- Punch through occurs at a lower voltage than gate oxide breakdown, so gates are protected.

Example: **PADOUT:** Inverter Chain: 3 stages,

each larger than preceding: Input 4x minimum, Next: (superbuffers) 4x preceding, Next: wide Enh. Mode FETS 8 times preceding.

Traded off max speed (xe) for simplicity, less area, lower power than the OM drivers/pads.

- **PADS: SIZE:** 126 μm (114 if overglassed).

BIG enough to be easy to Bond.

ELECTRICAL SIMULATION: Another Useful Design Aid.

p19-25 DICK LYON

- Very common use of computers in traditional unstructured IC design.
- However, for a small % of cells in our structured designs, electrical simulation can be very useful - to reduce delays and improve performance by varying design parameters & observing effects. EXAMPLES LONGEST CHAIN OF PASS-TR, NODE WITH HIGHEST FANOUT, CONTROL DRIVERS, OUTPUT DRIVERS.
- TWO WIDELY USED SIMULATORS: MSINC (SIMAG.) SPICE (BERKELEY) Tend to suffer from univ. Batch "card oriented" culture of design. Data Prep. is awkward. User interface poor. Not easily integratable in design systems.
- EXAMPLE: In Guidebook: Dick Lyon presents worked out Example of PADOUT OUTPUT DRIVER (SLIDE OF LAYOUT)
  - > Circuit Diagram of PADOUT is given (SLIDE) containing node #s, element names, W & L values for FETs.
  - > SPICE INPUT FILE, CALLED A "DECK", (SLIDE) indicates sorts of parameters required, EX: AS = area of source, AD = Area of drain. [Note: 1st inv not part of PADOUT. SIGNAL SOURCE 3.5v 20MHz SQ WAVE with 2 nsec Rise/falls + inverter combined external]
  - > OUTPUT PRODUCED IN LINE PRINTER FORM. (SLIDE) Node 1 to node 6 delay ~ 11 nsec @ T = .24 nsec [certainly optimistic] But helped very much to reduce delay relative to T.
  - > AT best such simul. only as good as their FET models & input parameters.

- GREAT NEED FOR & GEN. ABSENCE OF HIGHER LEVEL SIM.
  - > LOGIC TRANSFER FUN TESTS > R-R TRANS. SYS SIMULATION.
- All should be within same integrated design system, operating off same or machine generated variants of same data base, with att. paid to user interface. [BUT TRADE-OFFS VS IMPL TIME]
- Const. of such int. des syst. important requirement if [illegible] design is to be made more like "programming". [i.e. DON'T USUALLY SIM. PROGRAMS]

PRESENT MASK & FAB PROCEDURES
& HOW THEY AFFECT OUR DESIGN FILES / PREPARATIONS.

- (p 32-37) Contain Some More Details on Mskmaking.

Most Mask houses use GCA-Mann PG & Photorepeat Equip. The photorepeaters yield a limit to field exposable ~1cm²

Thus, we normally make ~~a~~ 10X reticles, and at most cover a 1x1 cm area on the wafer with these.

Now the package we use is std.d 40 pin - which will hold ~ 6mm x 6mm chip. So if use 1cmx1cm, must be able to scribe within it. (more later).

We must provide artifacts for:

> alignment marks used in fab sequence
> CD's used in mask making (lines of known width)
> scribe lines
> maybe "fiducials" used in photorepeating
> maybe "parity marks" used in photorepeating

We must also provide information regarding plate polarities, dep. on whether neg or pos resists used in fab line. etc. etc. etc.

- (p28-31) Contain More Details on Process

In particular: Quite a bit now precedes the first "oxide patterning" in our previous simple model of the process. Now, a so-called "Channel Stop" region is ion-implanted (pt) under areas where thick oxide is to be grown (rather than cut). This means we can use 2X DIFF-DIFF. It also cuts down on parasitic C's. (self-aligned)

But: the overall effect of the process is the same as that we've previously studied.

Note also: The substrate will be grounded. In packaging we'll use conducting epoxy to glue the chips into their package. Then connect gnd lead to package ground.

- ON: Now how do we deal with all these artifacts and procedures, etc. If each designer had to do all this, it would be an enormous overhead per design.
- Solution: Share the overhead via the Multi-Project Chip
- (CH 4 in text + p 51-67) TALK ABOUT BACKGROUND.

  SHOW SOME SLIDES OF PAST MPCS
- Only the "Coordinator(s)" have to know all the details. Individual designers just supply their design files.

- THE STARTING FRAME: If we exclude all the actual projects, we're left with the starting frame: all those artifacts which convey the projects thru MASK, FAB, & PACKAGING, & ELECTRICAL TESTING.

  > alignment marks > CDs > Fiducials > parity marks
  > scribe lines > electrical test patterns.

> SHOW SLIDES & DISCUSS

(see also cell library for CIF code of some of these artifacts)

> SHOW ALSO BLOWBACKS ON STAND

(PLOTS ALSO IN LAB)

INTERACTING WITH MASK & FAB FIRMS

- Assuming we will run GCA Mann PG, we must convert our CIF code to MANN PG format. This format is described on p. 74-78
- We must also provide the MASK firm with quite a bit of info, some of which is FAB line dependent. These issues discussed on p 38-40 and particularly,

  on p. 68, 69: [Copy of Specs sent to Mask house for the project set discussed in Guidebook.]

- **Discuss this SPEC sheet.**
- An Index of Manufacturers is Given p 72-73. Please use judgement here. Probably shouldn't contact unless you've got design file for project chip plus MONEY in hand.
- A large project set will cost ≈ 6k for masks, (mostly PG time), and ≈ 2k for FAB of ≈ 20 wafers. ~20 is a minimum run. If run more, less /wafer.
- We'll get enough chips so that every participant will have many chips to bond to just their project.
- Time: 3-6 wks masks, 3-4 fab, 1-4 misc.

MORE ABOUT TIME LATER: WE'VE GOT TO STREAMLINE ALL THIS, MAKE MORE LIKE PROGRAMMING. IF EVERYTHING WENT AS FAST AS POSSIBLE, WITHOUT QUEUES: DESFILE-CHIPS IN ≈ 3 days.

[ONE OF THE VERY IMPORTANT CHANGES COMING IS THE GENERAL AVAILABILITY OF FAST TURNAROUND IMPLEMENTATION]