LECTURE #11. 19 OCTOBER 1978

- Course Sched / Project Sched:

> I'll hand out a revised schedule next week sometime. Probably no more significant homework. But total of ~4 project assignments:

26 OCT: Tent. Project Selection
9 NOV: Detailed Proj. Desc: Blk Diag, Alg., Stick Dag of subsections.
21 NOV: Tentative Layout
7 DEC: Project Report

> I'll make selection for inclusion by 28TH NOV. Files Sent ~5 December.

> Selection: Will exclude: Those progressing slowly
Any with any obvious defects in des/layout.
Those not carefully subsetted for testing.

- RATE OF PROG.
- LACK OF SIGN. ERR.
- QUAL./NOV. OF APPL. OR DES.
- EFF. SUBS. FOR TEST

Will favor: Those completing early, well checked.
Interesting design or appl. concepts
Well subsetted for first testing

- I can arrange later to get full-size checkplots of entire project layouts for selected projects.
- Estimate that about 1/2+ the projects will get into the chip set (*)

- Would like to have a team formed to take on tentative design study for an important subsystem that will def. be done in LSI here later on: The Chaosnet interface. Like ~4 or 5 students to participate. This COULD be a very exciting project ... but also might be a hard one. Tom Knight & Jack Holloway of the AI Lab will be able to meet with a group next week to describe it, give handout on current MSI version. See Me After Class if interested. Personal Computing; Coax Comm. net; ---

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- MISC: Go over errors in Figs. in Ch. 5.

YIELD STATISTICS: HOW BIG SHOULD A CHIP BE?

- Empirically we find that as chip area increases, yield goes down; dramatically down

- There are no general, simple models. All we usually have is empirical data. But to get a feeling for the problem:

  [Suppose that defects are simple point defects, randomly scattered over the wafer, and that any single defect will kill a chip.]

  > Suppose there are N defects per unit area on average.

  Then the probable number falling within an area A is given (approx) by the Poisson probability: The prob that there are exactly n defects

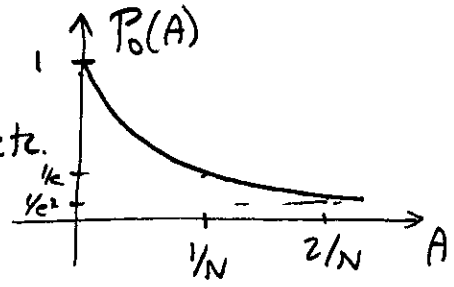
$$P_n(A) = \frac{(NA)^n}{n!} e^{-NA}$$

Data Analysis for Sci & Eng Meyer, Wiley Pub. '75

  In particular, $P_0(A) = e^{-NA}$ = probability of zero defects in an area A.

- Thus chips with $A >> \frac{1}{N}$ will almost never be found to work.

  chips with $A \sim \frac{1}{N}$ will have a yield of $\approx 37\%$, etc.



- In the real world of manufacturing, chip size thus is a highly complex matter, interacting with the cost of testing, the defect density, the part-type, etc., etc.

- Some Actual Values: Roughly, for big chips ~ 5mm x 5mm, yield will be ~ 10% or 50.

  A visual inspection finds 2/3+ of the defective chips. Testing finds the rest.

- Note: While our project chips are big, the projects are small, and yield will be very high, especially if inspected visually. If it doesn't work, it's probably a design error.

- We've Begun to Make analogies between integrated systems as hard patterned code and software systems as loaded code - i.e. the design, code generation processes, problems are really quite similar.

  BUT THERE IS ONE CRUCIAL DIFFERENCE: The integrated system compiler/loader doesn't produce exact identical copies of code: each chip may be slightly different due to defects!

  IMAGINE PROGRAMMING IN AN ENVIRONMENT where the loader Always tossed some random errors into your code! That's what we have to deal with in integrated systems.

- Maybe some clues about how to approach these issues could be gained by trying experiments with different ways of coping with such a software environment.

- Of course in big software systems, all the bugs are never out & people have learned some ways of structuring/testing to cope with complexity/errors. But in integrated systems you face this at the outset.

- AS WE SCALE DOWN TOWARDS VLSI, THESE ISSUES MAY BECOME VITAL. WE MAY BEGIN TO TRADE OFF FUNCTIONAL DENSITY FOR IMPROVED TESTABILITY... IF WE CAN GET ECONOMIC LEVERAGE IN SOME WAY -- i.e. MORE FCN FOR LESS OVERALL COST. COUNTING COST OF TESTING!

- EVEN BEFORE WE GET X100 DENSITY, WE CAN EXPLORE:
- WE CAN GET >X100 COMPONENTS INTEGRATED TOGETHER: HOW?
  USE THE WHOLE WAFER
- THIS WOULD NICELY "SIMULATE" VLSI (EXCEPT FOR T, POWER).
- **WHY ISN'T THIS DONE?** FIRST, I DON'T THINK ANYONE HAS REALLY TRIED. BRIGHT STUDENTS OF COMP. SCI/COMP. ARCH HAVEN'T STUDIED THE TECH UP TO NOW. MEANS OF IMPLEMENTING FULL WAFER DES. JUST NOW BEC. ACCESS (E-BEAM)

  Also, the industry doesn't take risks. It's always working on next years real product, and the process for the year after that.

- LETS TAKE A SPECIFIC EXAMPLE: YOU GUESSED IT: The Sorter!
  HOW DO WE COPE WITH DEFECTS. WITH TESTING:
  If we put many sorter sections on a wafer, each with some self-test circuitry, and with some type of bypassing interconnection form — we could **TEST THEM ALL IN PARALLEL, & STRING TOGETHER JUST THE GOOD ONES!**

  IDEAS EMERGING FROM SUCH EXPERIMENTAL ARCH/TESTING WORK COULD BE VERY IMPORTANT IN FUTURE VLSI.

- SO LETS THINK BIG! NOT ONLY WILL WE GET MORE DENSITY (MUCH MORE), AND FASTER DEVICES, AND LOWER POWER PER DEVICE. BUT WE CAN GET BIGGER CHIPS! IF WE COULD PARALLEL TEST/CONFIGURE

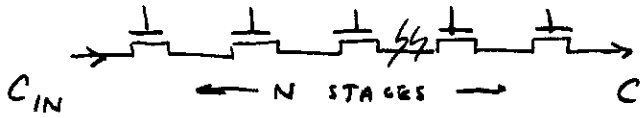
AH! BUT DON'T GET TOO CARRIED AWAY: BE CAREFUL: YOU'VE GOT TO GET LEVERAGE:

EXAMPLE: At a module yield ~ 1/2, For area A, if double A to get self-test + connection net, then yield → ~1/6.

So if start with 100, get only 50 (@ 2A per) of which only 1/6 th now work ~ 8 equiv chips. [Play with the number of sections]

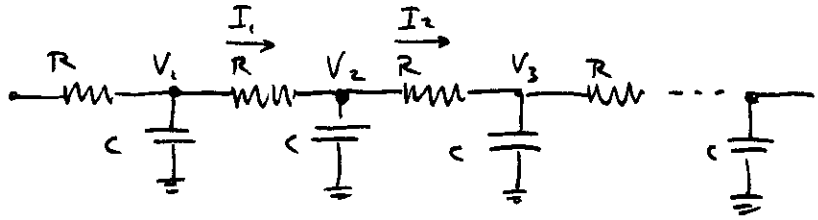
ANOTHER TOPIC: DELAYS IN PASS TRANSISTOR LOGIC

- WE KNOW THAT DELAYS IN INVERTING LOGIC GO AS $O(N)$
- BUT WHAT ABOUT "SWITCH ARRAYS" OR "CARRY CHAINS" IMPLEMENTED USING PASS TRANSISTORS? HOW DO THESE COMPARE?
- CONSIDER:



QUESTION: HOW DOES DELAY GO AS FCN OF N?

- APPROX EQUIV CKT:



[MIN R = res of on pass-trans, min C = min C_g. Parasitics increase these values, especially C.]

- Consider $V_2(t)$: $C\frac{dV_2}{dt} = I_1 - I_2 = \left[\frac{V_1 - V_2}{R}\right] - \left[\frac{V_2 - V_3}{R}\right]$
- If we considered R & C per unit length, then this reduces to differential form:

$$RC\frac{dV_2}{dt} = \frac{\Delta V_{1-2} - \Delta V_{2-3}}{\Delta x} = \frac{\Delta^2 V}{\Delta x^2}$$

ΔV_{1-2} = change in V for change in x; ΔV_{2-3} = change in V for change in x; $\frac{\Delta^2 V}{\Delta x^2}$ = change in $\frac{\Delta V}{\Delta x}$ for change in x

$$\boxed{RC\frac{dV}{dt} = \frac{d^2V}{dx^2}}$$

Where: R = res/length
C = cap/length

Slide

- This is the well known Diffusion Equation.

  Its solution are complex, but in general the time required for a transient to propagate in such a system is proportional to X^2.

- This can be seen qualitatively: Doubling N doubles both R & C in the system, multiplying an inherent time constant by 4.

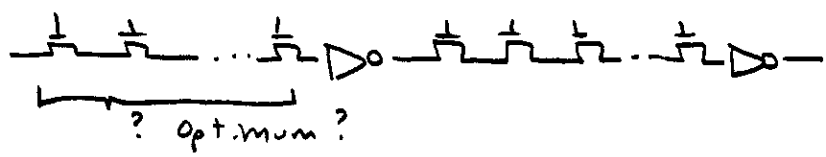
- ∴ One extra pass transistor: Adds little delay to a small chain

  But may add a lot of delay to an already large chain!

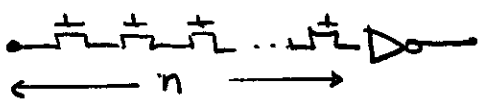
- WHAT TO DO! Aha! **Break up long chain into sections Put inverters in between**

Accept/Trade the added fixed delay for big reduction in the overall total delay!

- HOW OFTEN?



- SUPPOSE HAVE:



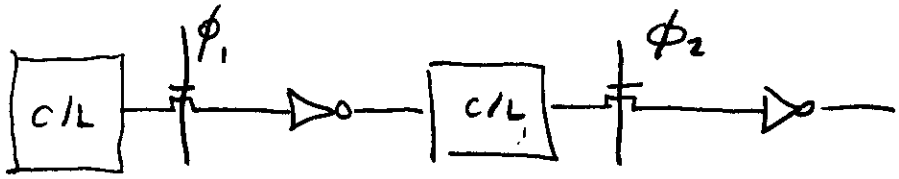
- TOTAL DELAY $\cong RCn^2 + T_{inv}$
- AVERAGE DELAY/STAGE $\cdot RCn + T_{inv}/n = f(n)$
  we find that minimizing f(n), the min occurs when: $\boxed{RCn^2 \sim T_{inv}}$ So thats how to choose n
- Right now: $T_{min}\, n^2 \sim T_{inv} = \frac{9}{2} \cdot 2\, T_{min}$, ∴ $n^2 \sim 9$

  and $\boxed{n \sim 3}$. We'll usually use $n \sim 4$
- IN CLOCKED STAGES: (IT'S AN ARCHIT. QUESTION. CAN USE UP TO THE MAX DELAY ON A Φ WITHOUT PENALTY)

TRANSIT TIMES & CLOCK PERIODS

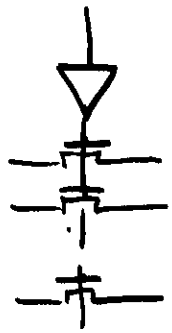
- What is the shortest clock period we might be able to use in 1978 for synch. digital system in nMOS?

Consider:
R-R Transfer stage



- NORMALLY THE C/L + CLOCK GATE: IN PASS TRANSISTORS.
- Level Restoring will be inverters: $k \sim 8$. Max dly $\sim 8\tau$
- NORMALLY THESE will be MATCHED:
  C/L + CLOCK: $\sim 8\tau$, INV. MAX $\sim 8\tau$
- THUS TOTAL OF $\sim 16\tau$ per phase $\times 2$ for STRAYS.
- THUS $\sim 30\tau$ per clock phase.

> BUT CTL lines typically drive 10 to 30 pass transistors.



- Even if SUPER BUFFERS, if $Y \sim 30$, Driver delay is $\sim 9\tau$
- MUST ADD $\sim 8\tau$ to operate drivers

> $\therefore$ Total Clk $\phi \sim 50\tau$, $\therefore \boxed{T \sim 100\tau}$

- In 1978: $0.3 < \tau < 1.0$ ns so $T \sim 30$ to 100 ns.
  (For compact synch. d.j. syst)

However, if some signals must run for long distances, drive very large loads, or are gated by longer pass-T chains, the corresponding ϕ_i and thus T will be longer.

For example in OM2, ϕ is 50τ but ϕ_2 has a delay of 100τ for each 4 bit ALU block, so $\phi_2 \sim 400\tau$.
$\therefore \boxed{T(OM2) \sim 450\tau}$ or (135 ns to 450 ns = few MIPS)

(*) UPDATE ON RULES OF THE GAME:

Area Estimates: Negotiating for Area (AKA "SPACE WAR")

36 people will participate in projects

Possibly: 4 - 3 pers, 6 - 2 pers, 12 - 1 pers = 22 tot. projects.

likely ~ $1/2^{+}$ to $2/3^{-}$ will get done/look o.k. to go on chip set.

So probably: ≈ 12 - 15 projects will go on chip.

Chip set likely to be 6 mm x 10 mm (2 chip types).

Area ~ 60 mm^2. Probably ~ 10 mm^2 will go for scribe lines, alignment marks, test patterns, etc. Maybe a bit more for "packing inefficiency".

So: maybe 45 mm^2 / 15 projects = 3 mm^2 / project.

So: A large project will be 2 x 2 mm = 4 mm^2.

If we put many of these, or some bigger ones, they'll have to be compensated for with some little projects.

Try for 2 mm^2	Let me know early if you'll want to go over 4 mm^2

> USE SYMBOL # 100 or greater
> The Lib. will use symbols 1-99

[redacted]: Priorities? CIF Cell?