## Foreword

During the past several years, the LSI Systems Area of Systems Science Laboratory (SSL) at Xerox Palo Alto Research Center (PARC) has conducted research in the architecture and design of integrated systems. One focus of that research, in collaboration with the Caltech Computer Science Department, has been the exploratory development of new design methodologies that simplify integrated system design.

Through this research, new design techniques have evolved and been debugged; these techniques can be more quickly acquired and more widely practiced by system designers than was possible in the past. It has been a period of discovery and iteration, moved forward by courses taught to university EE/CS students in which the students undertook LSI design projects as part of their class work. This process has lead to the publication of the textbook *Introduction to VLSI Systems* [Mead & Conway 1980] describing the new design techniques.

In order to make possible an "acid test" of the evolving design methodologies and of the resulting student designs, a parallel effort has been conducted in SSL to investigate, understand, simplify, and make more efficient the procedures for the *implementation* of LSI design projects. The term "LSI implementation" is defined here as the series of all tasks involved in going from a set of LSI design files to a set of packaged chips ready for functional testing. Implementation thus involves collecting and merging design files into starting frames, converting the merged files into patterning format, making masks, fabricating wafers, and packaging the resulting chips.

Bob Hon and Carlo Sequin have played leading roles in the SSL LSI implementation activities. They originated many of the new standards and procedures, and then validated these techniques while carrying out the implementation of several multiproject chip sets. These implementation activities have led to the discovery of new techniques that greatly reduce both the overall time for implementation and the cost of implementation per design project. Practical methods have been developed for simplifying the interfacing of design groups with mask making and wafer fabrication firms. A standard design-interchange format (CIF 2.0) has evolved from an early Caltech format and is now in widespread use in the universities and industry. All these and more are the subject of this report.

Bob and Carlo are to be congratulated on the success of these efforts and on the production of this timely and useful report. Only those who were near the action can visualize the imagination required and effort invested to reshape the "Silicon Valley folklore" concerning LSI implementation into a comprehensive, general, compact, and straightforward body of knowledge. Their work has been a key factor enabling the rapid spread of the participation of university students, faculty members, and researchers in the new field of VLSI system design.

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18 January 1980