CHAPTER 6
AN EXAMPLE STARTING FRAME AND PROJECT CHIP

The starting frame and test patterns described in sections 6.1 and 6.2, respectively, were implemented on a multi-project chip during the summer of 1978. That chip contained ten projects, ranging from process test structures to novel arithmetic and memory circuits. Figure 6.1 shows the overall layout and one mask layer of the chip. The chip includes a set of alignment marks and line-width testers laid out by Bob Hon and Dick Lyon and a general process test chip laid out by Rick Davies.

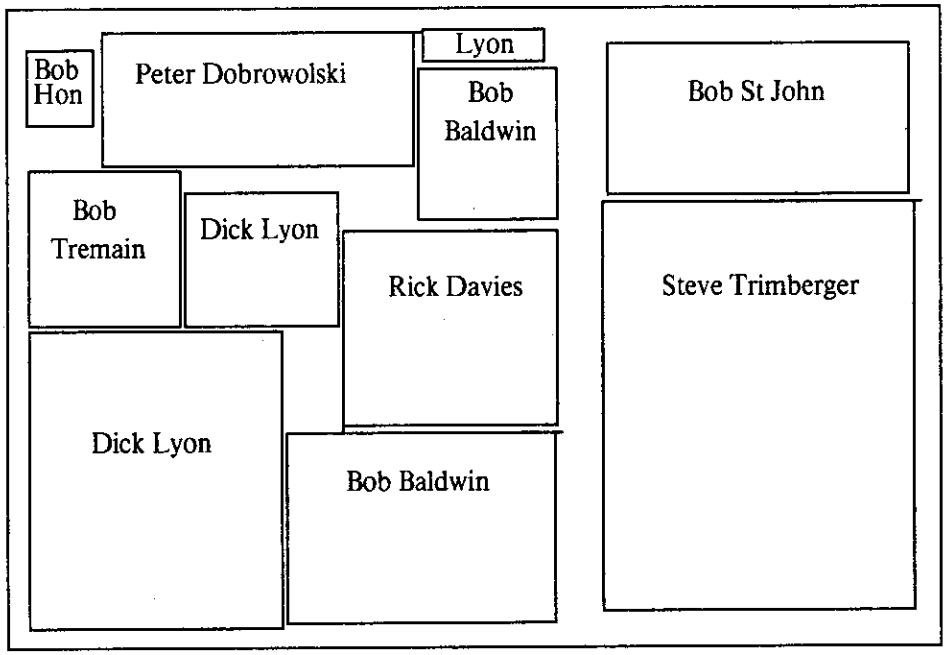
In this chapter the features of the starting frame are presented first, followed by a discussion of the general test chip. Finally in section 6.3, Jim Cherry, a graduate student at MIT, details a project that he designed for a course given there in the fall of 1978.

6.1 The PARC Starting Frame

The multi-project chip is divided into two parts separated by one internal scribe line so that both parts are small enough to fit inside the cavity of a 40 pin DIP. Further, the layout is enclosed by exterior scribe lines placed around the periphery. The exterior lines differ from the interior lines in that the former are missing the outside "shoulder" (Figure 6.1.1); the exterior lines of one pattern are completed by the overlap with the exterior line of the next chip. The scribe lines are designed to provide direct access to the Si substrate for the scribe tool during wafer separation (see section 5.2).

The alignment marks (Figure 6.1.3) were intended to unambiguously indicate which layers are to be aligned relative to each other. The marks consist of a number of "squares" and "fortresses". A square mark is placed on those layers that will serve as reference layers for masks in following fab steps. Each square has a corresponding fortress, located on a different mask, which will be aligned over it during the appropriate step (see Figure 6.1.2). Each layer includes a large rectangle around all of the alignment marks to help the operator to locate them and to insure that the sequence is not shifted. The features are lines rather than areas, permitting the operator to align edges relative to one another. This makes the marks usable for clear as well as dark field working plates.

The fortress/square pairs are used in a left to right progression; a digit (omitted in the figures below for clarity) is placed in each fortress to indicate when it is to be used. A fortress is always aligned over a square and there is never more than one fortress per mask. The alignment sequence has the depletion mode implant, buried contacts (when used), and the polysilicon layer all aligned relative to the diffusion layer. The contact cuts are aligned relative to the polysilicon since there



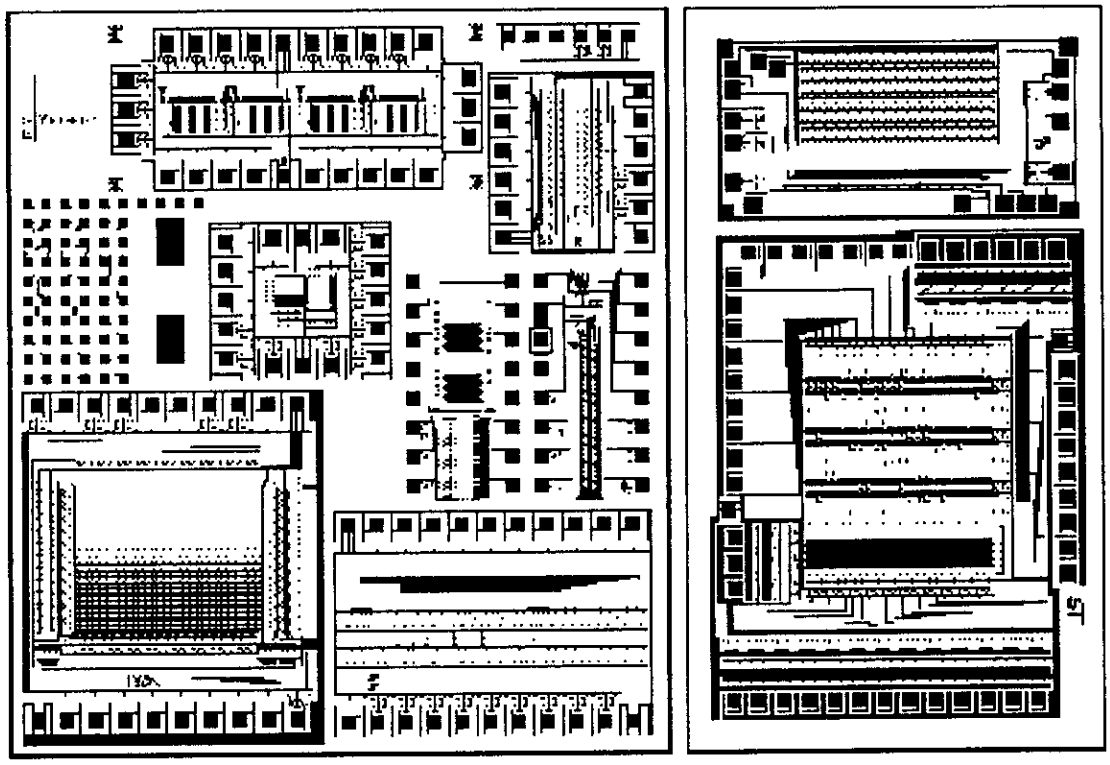
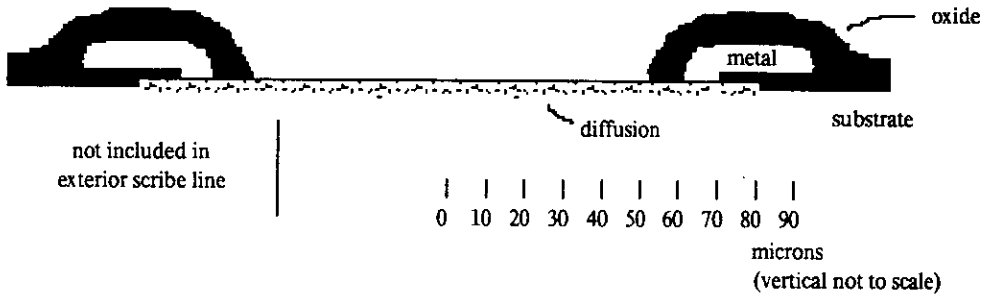


Figure 6.1 The Summer 1978 PARC Multi-Project Chip

Figure 6.1.1 Scribe Line Profile



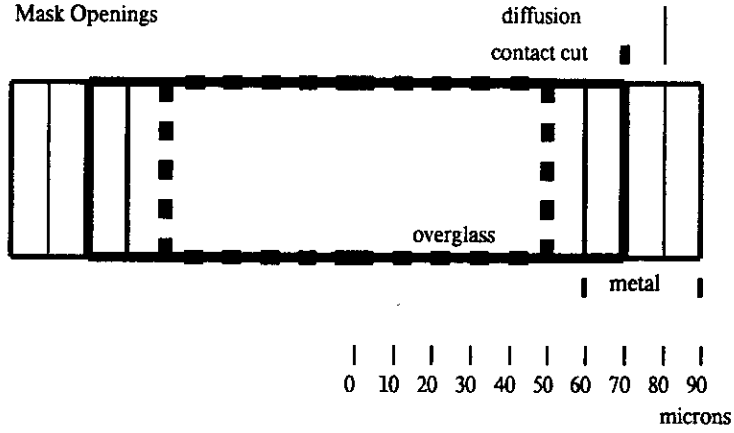
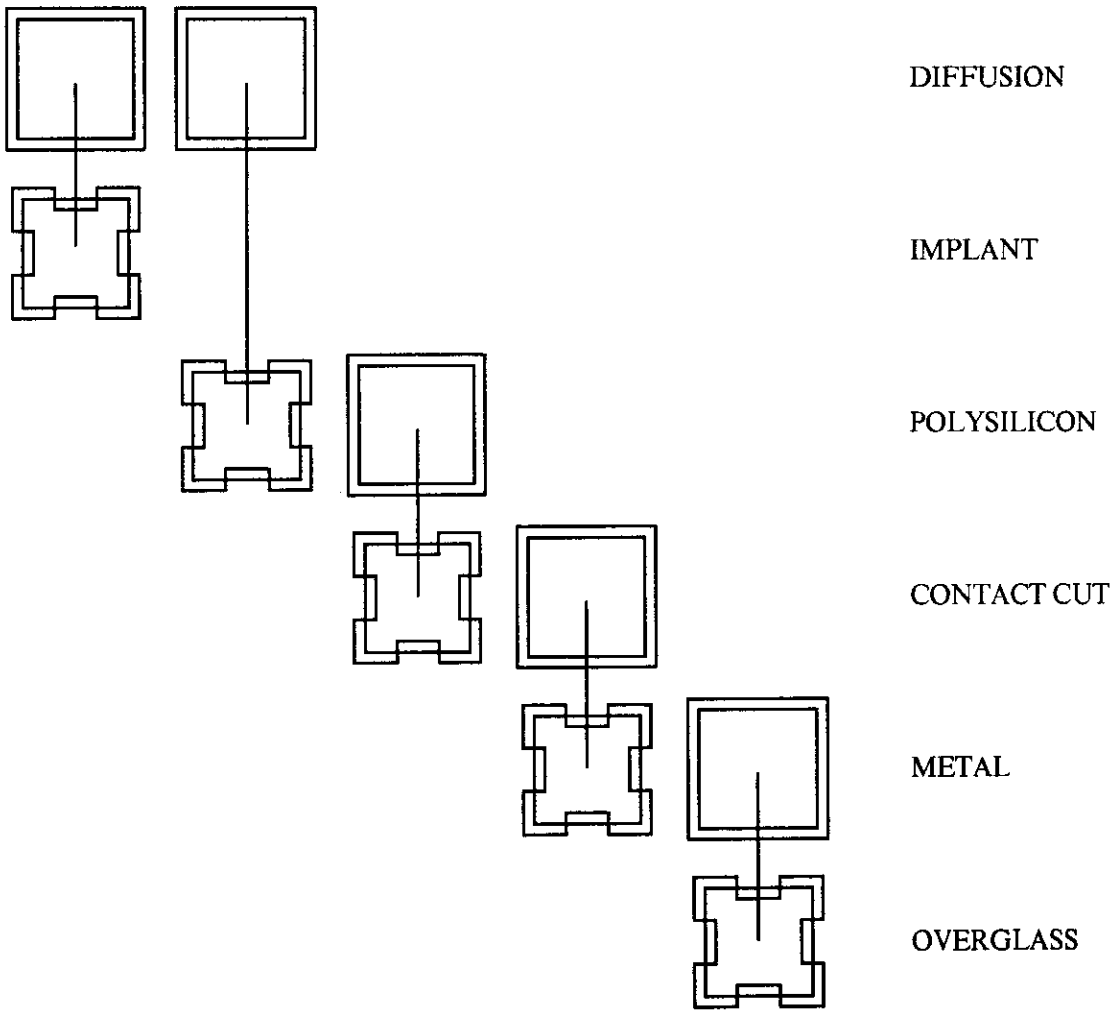
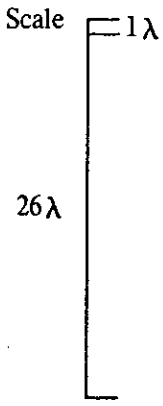


Figure 6.1.2 Alignment Marks for Mask Layers





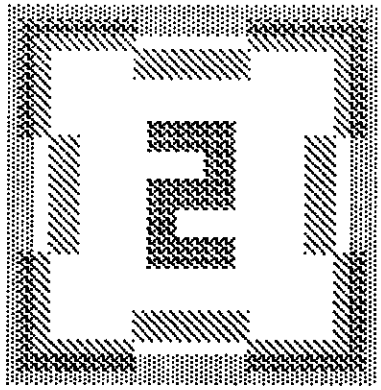


Figure 6.1.3 Alignment Mark

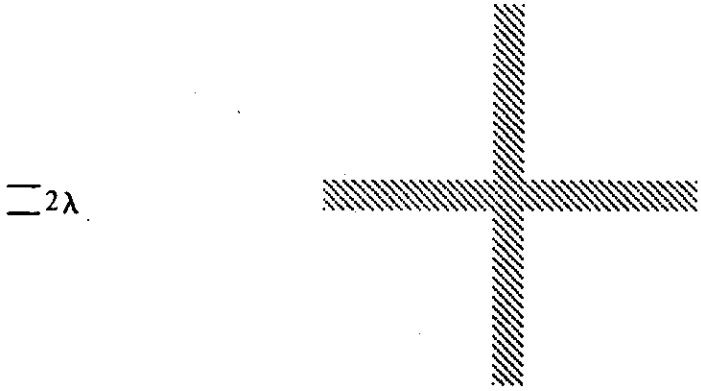


Figure 6.1.4 Critical Dimension Cross

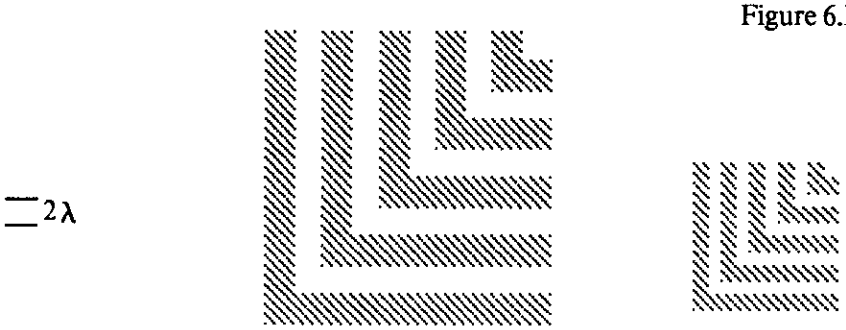
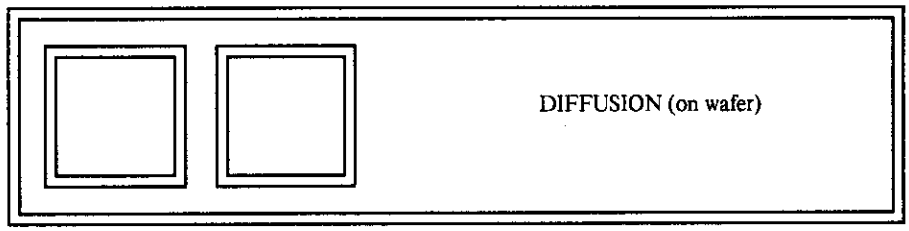
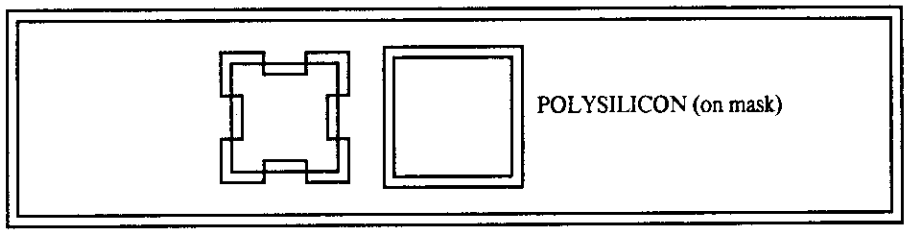


Figure 6.1.5 Etch Test Patterns

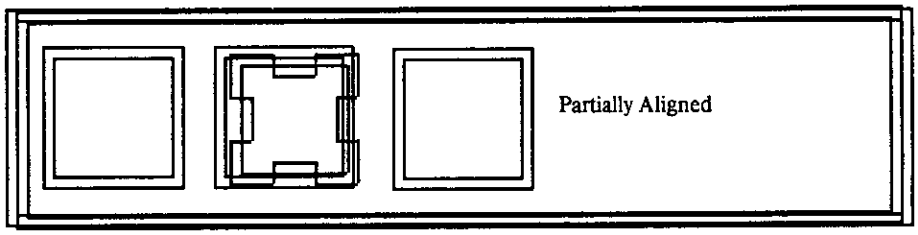
appears to be more tolerance to misalignment between contact cuts and diffusion. The metal aligns to the contact cuts and the overglass to the metal layer. The following illustration represents the way an operator might align the mask for the polysilicon layer to the wafer. The pattern on the partially processed wafer is:



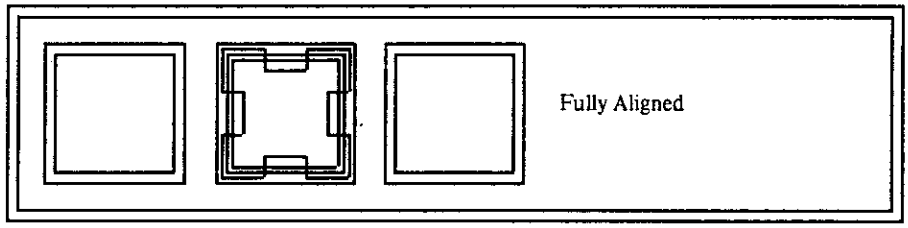
The operator must now align the polysilicon mask, which contains one fortress and one square.



The diffusion and depletion implant steps are already complete, thus the first fortress/square pair has been used. The operator lines up the second pair using the gross alignment mark for guidance. The following diagram shows the mask in partial alignment with the features in place on the wafer.



Final corrections are made using the fortress/square pair.



The third square will be used to align the contact cut layer; a fourth square is placed on the wafer during the contact cut step and will be used to align the metal layer.

The critical dimension marks are simple crosses made of lines (Figure 6.1.4). The line widths vary from layer to layer, and are typical of the feature dimensions found on the particular layer.

A set of features used to monitor the quality of the working plates and fabrication process was also included. This *etch test pattern* (Figure 6.1.5) consists of a set of nested "L"'s with the same spacing between L's as the width of the feature; two different sizes were included on each level to check the quality of the mask and the quality of the photolithographic process.

Measurements on each mask layer provide a check on the dimensional correctness of the working plates while measurements on the wafer are used to verify that the fab line performed as anticipated (e.g. that lines over- or under-etched as expected).

Appendix A contains a copy of the information sent to the mask house.

6.2 Test Patterns

[contributed by Rick Davies, Xerox PARC]

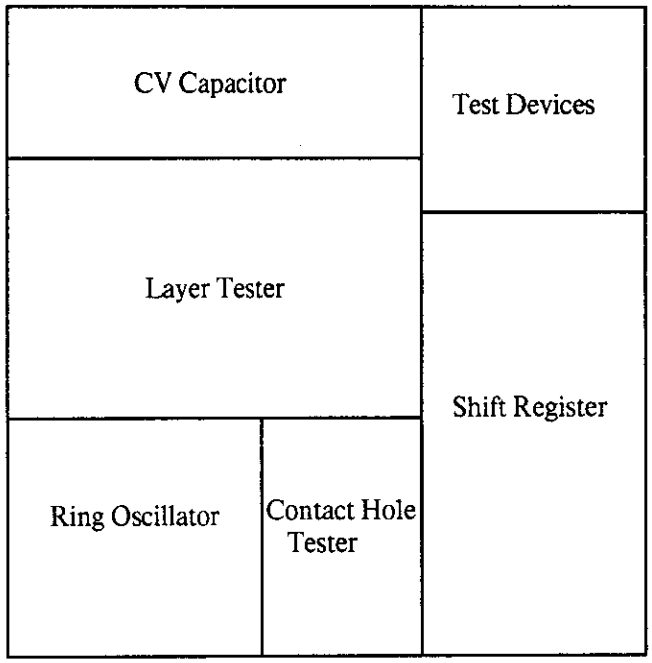
The starting frame contains a number of simple test structures to answer the following two questions:

> Was the wafer properly processed? Specifically are all the layers properly patterned, are gate oxide and deposited oxide films of acceptable dielectric integrity, are contact holes properly opened, etc.?
>
> What are the first-order device and circuit performance characteristics such as transistor threshold voltages, extent of short- or narrow-channel effects [Dennard 1974, Wang 1978], polysilicon sheet resistivity, and inverter propagation delay obtainable with the process?

The test structures described here are general enough so that it is assumed that they will prove useful to most participants in a multi-project chip. This should not deter any designer from adding his own special test structures. It may be desirable in the future to add additional patterns to the common test structure, to test such parameters as the quality of the buried contacts between

diffusion and polysilicon or the limits of wafer processing (e.g. At what spacing do metal lines begin to show bridging?).

The test pattern consists of several separate regions which are described below. It occupies 2 mm x 2 mm and has this general layout:



6.2.1 Layer Tester (Figure 6.2.1)

This is a long serpentine metallization path that runs between two interdigitated metal combs and lies over a serpentine of polysilicon and active transistor area. It tests the following features.

Metal bridging. There is an 8400λ periphery of minimum-spaced (3λ) metal lines between the serpentine and combs. Conductance between the serpentine and either comb indicates bridging, which could be caused by improperly patterning the photoresist or incompletely etching the aluminum.

Metal step coverage. The 4λ-wide serpentine passes 266 times over a 2λ-wide region of polysilicon, over gate oxide, between 2λ-wide source-drain diffusions. This should provide a good indication of step-coverage quality (assuming that the above bridging test has been passed), measured as a low end-to-end impedance (<100Ω). Metal running over diffusion and polysilicon is the worst-case condition for metal step coverage; the limited solid angle provided by the evaporation source can make it difficult to deposit aluminum on the vertical features in small-geometry devices.

Gate-oxide dielectric integrity. A polysilicon electrode of approximately $11{,}000\lambda^2$ over gate oxide provides a test for pinholes and shorts between gates and transistor-channel area. This is equivalent to the gate area of about 1000 transistors of typical size. To pass this test there must not be measurable conductance between the polysilicon and the diffusion.

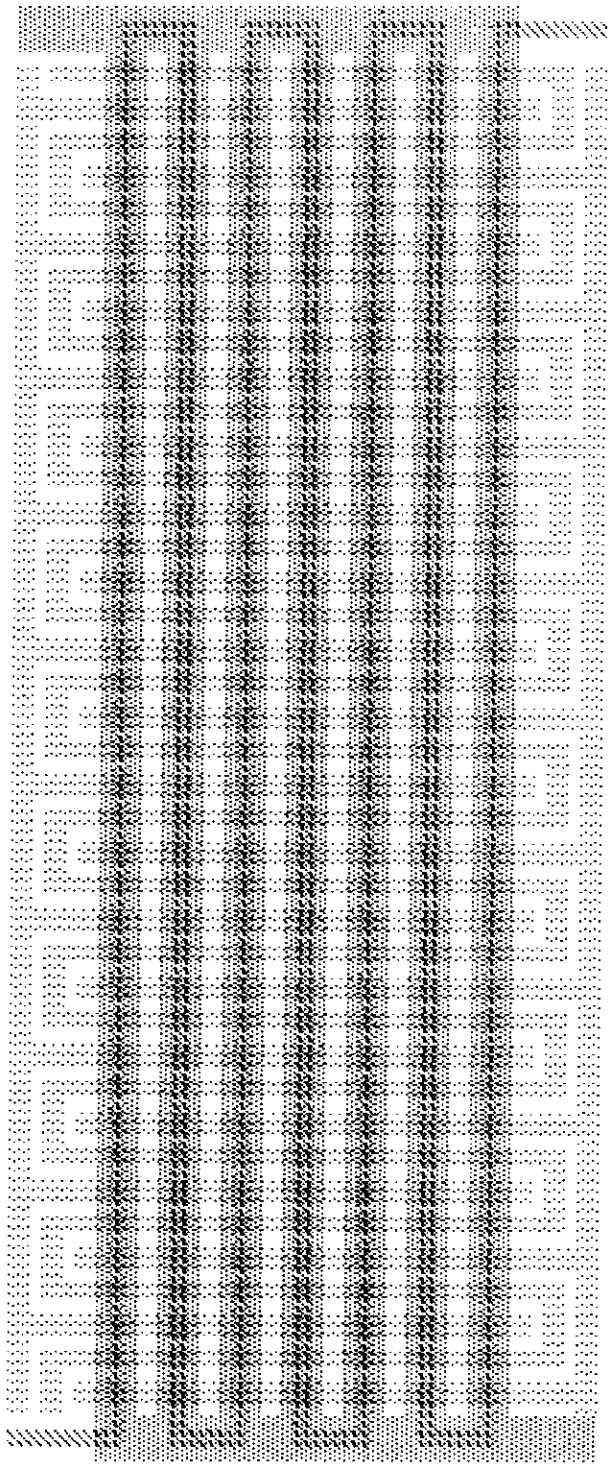


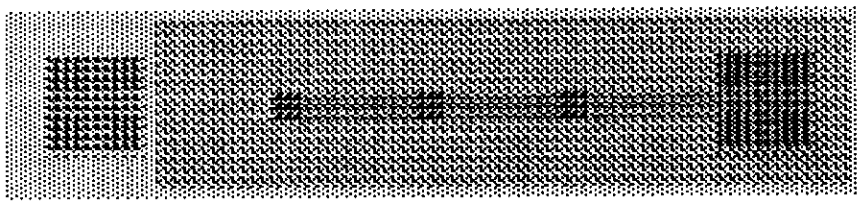
Figure 6.2.1. Layer Tester

Deposited-oxide dielectric integrity. The presence of approximately 11,000λ^2 of metal over active area (polysilicon gate or source-drain diffusion) provides a test for pinholes and shorts to the metallization; this could result from improper annealing of the metal causing spiking through the deposited oxide layer. No conductance should be observed between the metal and either diffusion or polysilicon.

Polysilicon and aluminum sheet resistivity. Although more accurate resistivity measurement can be made using a Van der Pauw structure (separate forced-current and sensed-voltage terminal pairs), polysilicon and aluminum serpentines provide a quick estimate by inspection of the end-to-end resistance. About 700 squares are present in either level.

6.2.2 CV Capacitor.

A 68λ x 289λ MOS capacitor with a diffusion guard-ring is provided for analysis of the process parameters Q_{SS} (density of fixed charges at the oxide-silicon interface), N_{SS} (density of trapping states at the interface) and the gate oxide thickness [Grove 1967]. A minor amount of wafer preparation may be required to form a suitable ohmic backside substrate contact for reliable measurements.



Measurements on this structure would allow separate determination of the implant dose and interface characteristics components of the threshold voltages of the enhancement and depletion NMOS transistors. This structure may also be used to test gate oxide dielectric integrity; 20,000 λ^2 are present.

6.2.3 Contact Hole Testers

The following two contact-hole tests are incorporated on this test pattern (Figure 6.2.3).

A series connection of 270 metal/polysilicon contacts (2λ x 2λ) tests for failure to make electrical contact between metallization and the underlying layer. A measured resistance significantly above the expected impedance corresponding to the parasitic 135 squares of connecting polysilicon indicates poor quality ohmic contacts. This could be caused by improper imaging of the pattern in the photoresist (in particular a scum residue might have been left in the bottom of a hole), improper etching of the oxide, or by metal breakage around the rim of the etched contact hole.

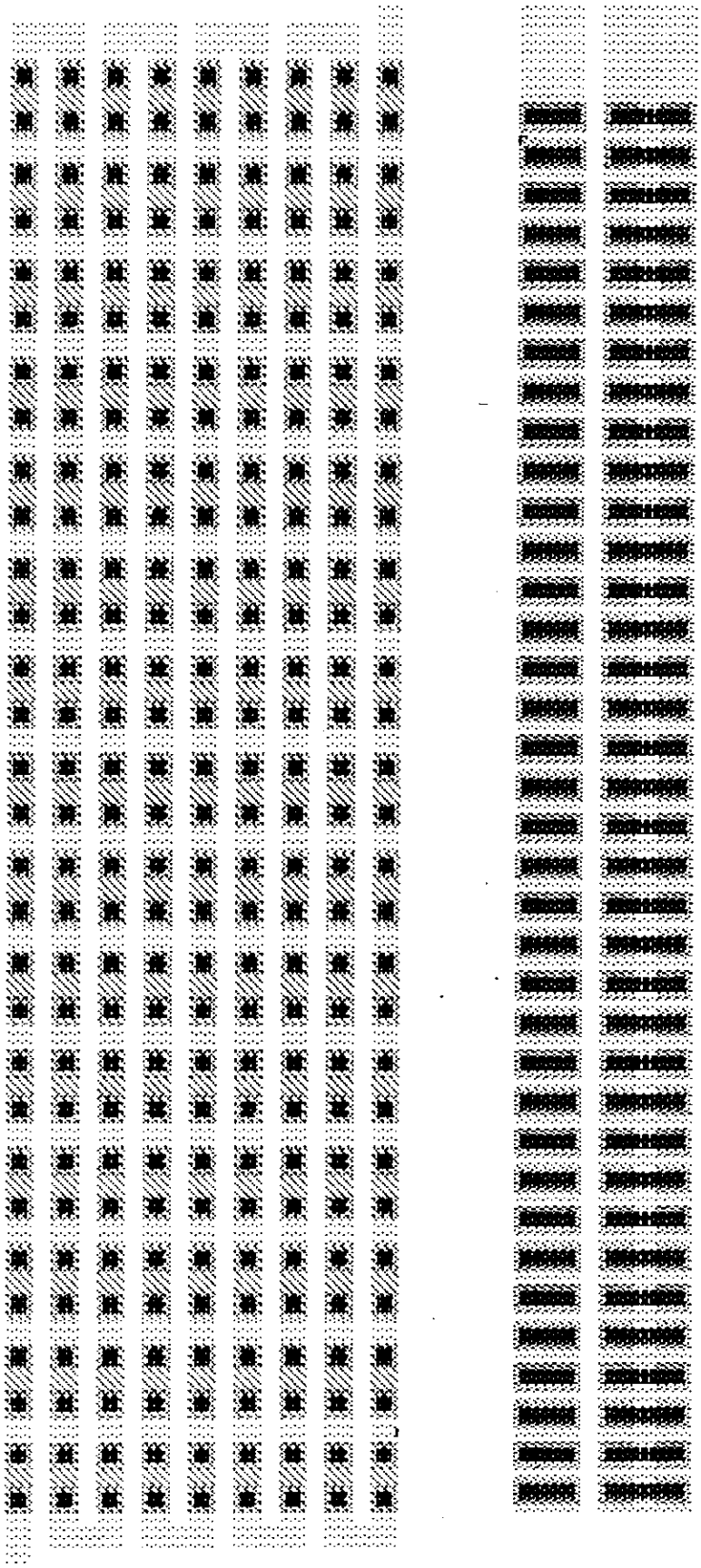


Figure 6.2.3
Contact Hole Testers

A special tester consisting of 2 columns of 36 metal/diffusion contacts compares contact holes that are properly centered over a diffused area and others that overlap the field oxide region. The latter is used to test whether one could overlap contact holes onto the field oxide, in order to save the area otherwise consumed by alignment tolerance. Because the phosphorus-doped SiO_2 (sometimes called *P-glass*, see section 3.3 for a description of the fabrication process) deposited before contact hole definition etches much faster than does the thermally grown field oxide, the contact holes should open before the field region is etched through.

The two columns have identical bottom-wall diffusion area, diffusion periphery, and contact hole area over diffusion; the right one differs from the left only by the incorporation of a strip of field oxide in the middle of the contact hole. If the two columns reveal the same leakage characteristics to the substrate, then this overlap technique is probably acceptable.

6.2.4 Discrete devices

Four enhancement and four depletion mode transistors are provided for dc testing (Figure 6.2.4). They are organized as four inverters for convenient transfer curve analysis, with uncommitted gates for the depletion-mode transistors to allow full testing of those devices. To minimize the number of bonding pads, the enhancement-gates are shared, as are the depletion-gates; all enhancement-sources and all depletion-drains are also shared. The four inverters are:

2λ-length/4λ-width enhancement NMOS with 4/2 depletion NMOS, forming a standard 4:1 inverter.

2/4 enhancement and slightly narrowed 3.3/2.5 depletion load device. One expects a higher threshold in the narrowed channel because the channel potential is raised by the increased influence of edge effects. The use of scaling [Wang 1978] (which involves altering the fabrication process) would permit this smaller layout without disturbing the dc characteristics.

2.5/3.3 enhancement and 4/2 depletion load devices. Short-channel effects should cause a lowering of the threshold voltage and produce increased output conduction in the enhancement device [Dennard 1974].

20/40 enhancement and 40/20 depletion load devices. These devices should permit one to check device characteristics with little interference from peripheral effects.

Two transistors with closed layouts — one with a metal and the other with a polysilicon gate — on thick field oxide, are provided to test for isolation-region channeling or other parasitic leakage. A threshold voltage above about 25v should exist on each device. In both cases the transistor gate electrode overlaps the source and drain regions. The poly-gate structure makes gate-oxide devices at source and drain that are in series with the field-region under test.

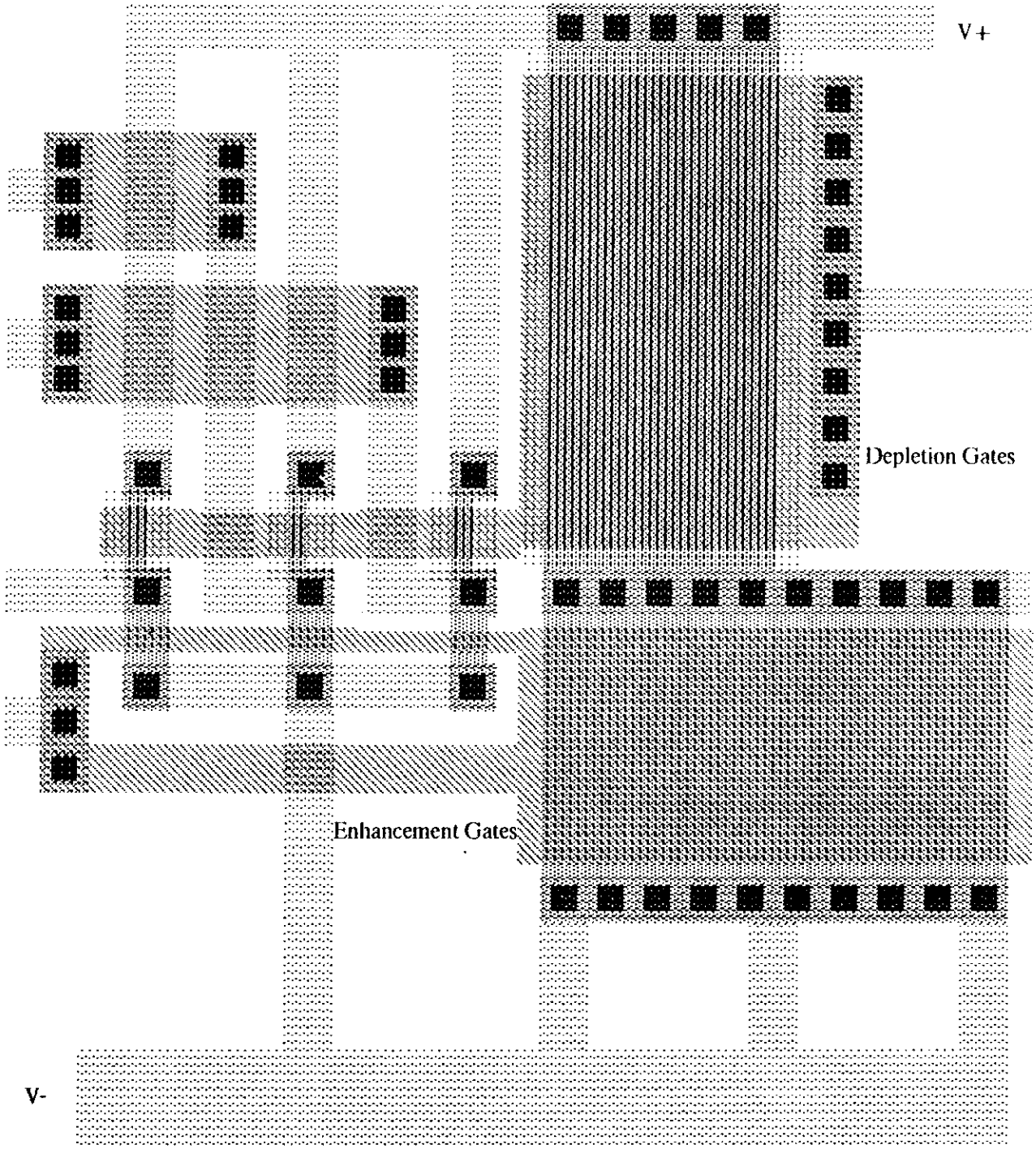


Figure 6.2.4 Discrete Devices

6.2.5 Ring Oscillator

This structure tests ac device performance in a probe environment without hindrance from the inherent parasitic capacitances. Because it is an actual circuit, it should provide more reliable and directly usable information than that derived from separate detailed ac device measurements and circuit simulation techniques. The ring oscillator is 25 stages long to provide a low frequency output signal. The average propagation delay is one half of one twenty-fifth of the inverse of the natural loop oscillation frequency. Inverters with $2\lambda/4\lambda$ enhancement drivers and $4\lambda/2\lambda$ depletion loads are used; a buffer/inverter taps the loop, giving one of the 25 loop inverters a fanout of two. The buffer in turn feeds an output transistor with L/W of 1/20; this may be used either as a common-source output driver or as a source-follower.

6.2.6 Shift Register

This 33-stage circuit is similar to the above ring oscillator, with the addition of a passgate in front of each inverter (they are $2\lambda/8\lambda$ enhancement drivers and $4\lambda/2\lambda$ depletion loads; the passgates are $2\lambda/2\lambda$ devices). The passgates are bussed in two phases that alternate between inverters (16 passgates per phase). The 33rd passgate is brought out to a separate bonding pad so that one can open the shift register loop. The complement of this signal is applied to another passgate that connects the shift register to a separate, inverting input buffer.

With both passgate phases and the control passgate line high, the circuit implements a 33-stage ring oscillator using passgate signal transmission. The measured average propagation delay may be compared to that of the simple ring oscillator (described in section 6.2.5).

With the control passgate line low and alternate clocking of the passgate phases, the circuit acts as a shift register which may be loaded with an arbitrary bit pattern. Raising the control passgate line while continuing two-phase clocking (at a rate below that of the loop self-oscillation frequency) forms a recirculating shift register.

6.3 Example Project: A Transformational Memory Array

[contributed by James J. Cherry, MIT]

6.3.1 Background and Abstract

In this section the design of an LSI chip will be described from its inception through the selection of the architectural structure and on through final layout, to illustrate the integrated nature of the process. The selected example is as one of the projects produced during the 1978 VLSI design course taught by Lynn Conway at MIT. It is a special purpose NMOS memory array for use in an object oriented graphics display. The memory is an 8x8-bit array which may be non-destructively accessed in serial-raster scan format. This bit map can be read in its original orientation, mirrored about the X or Y axes, and/or rotated a multiple of 90 degrees.

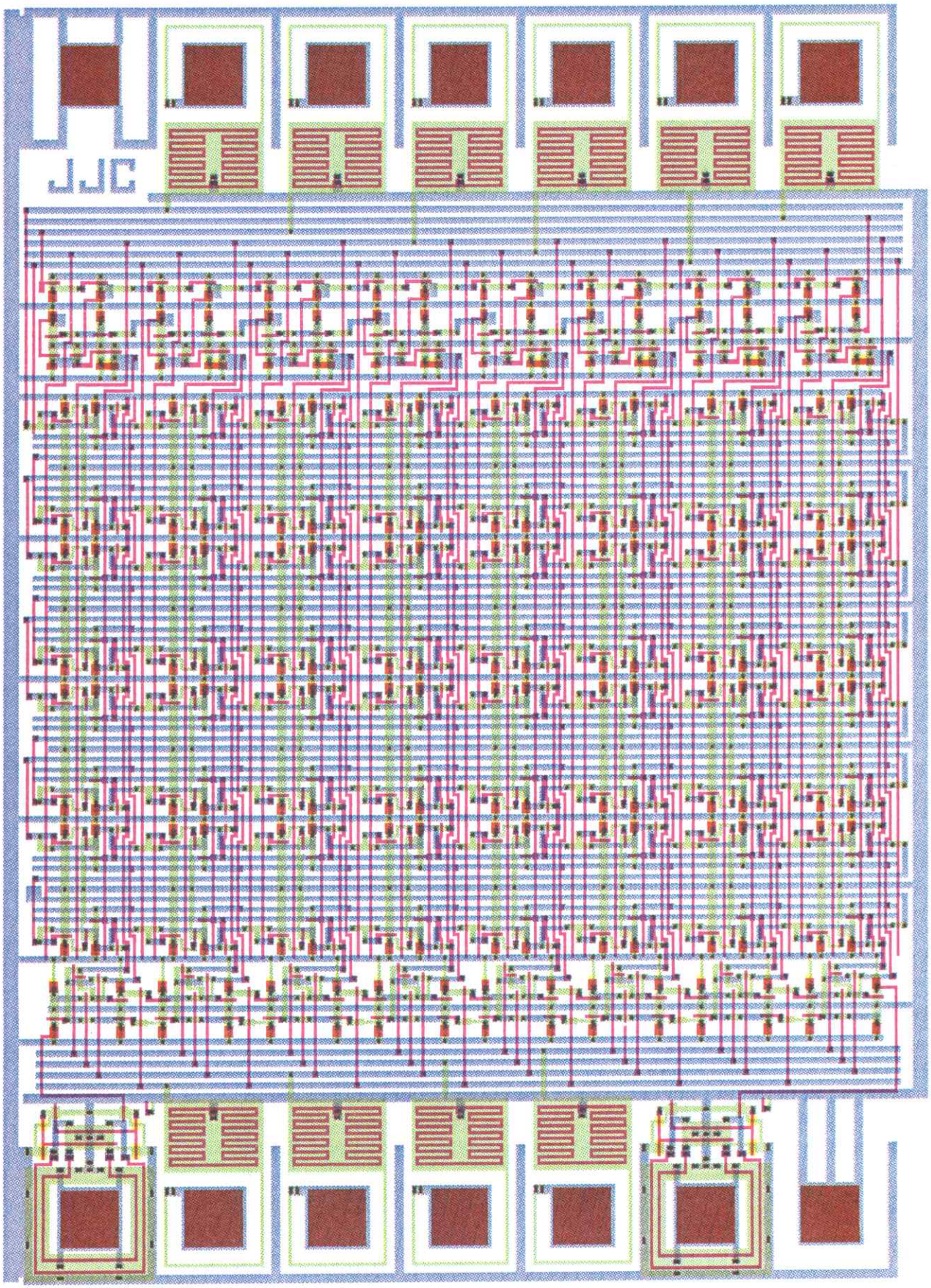
6.3.2 Project Context

In many video graphics applications, a display may have a variety of logically distinct objects. It may be desirable to have the capability of placing each object at an arbitrary orientation and position on the screen. An example is a game in which space ships or cars move under user control. In addition to moving across the screen, it is desirable to have the vehicle point in the direction it is moving.

While this may be accomplished using a bit map storing the pixels on the entire screen, operations such as those mentioned above require a lot of computation. Even the translation of an object is difficult, since an object will most likely change its position relative to the word boundaries when moved. To perform mirror images or 90 degree rotations, requires an even larger number of bit manipulations.

In the context of logically distinct objects, the hardware could be made to follow the structure of the objects to be displayed. In other words, create hardware that is specialized to display a single object, where each module is as intelligent as hardware limits permit. For instance, the module may know the coordinates of its upper right hand corner. As the display is raster scanned the modules act as demons, waiting for the addresses which correspond to its region to send their content to the display. This makes the translation of an object a simple matter for the processor. It merely updates the corner register's contents. The outputs from a number of modules can then be ORed together to form a composite display. A fixed pattern (background) may also simultaneously appear by ORing in its contribution.

Associated with each module may be a variety of attributes. Examples include transformations performed on the pixel matrix such as mirroring in X or Y and rotation. The color of the object may also be considered an attribute. A collection of these modules allow a number of objects to be simultaneously displayed. This frees the processor for higher level tasks.


JJC

6.3.3 Project Scope

The above module can only be useful if a several of them (one for each separate object to be displayed) are available. To implement even the simplest hardware module, capable of displaying a single object in its original orientation, requires on the order of fifteen TTL packages. This renders the approach quite uneconomical when implemented with off-the-shelf SSI/MSI integrated circuits. Only, if the module itself is implemented in a single IC, the approach becomes reasonable. To be truly useful the modules should be smart enough to perform localized operations on the data itself. Mirroring and 90 degree rotations are almost required transformations. Rotations through arbitrary angles do not have simple mappings from the original to the transformed bit map, and are thus very difficult to implement.

The chip to be described is an (8x8)-bit memory array that is read in raster scan format suitable for use with a video monitor. The bit map array can be read in its original orientation, mirrored about the X or Y axes, and/or rotated a multiple of 90 degrees. I have decided not to implement the coordinate detection logic, primarily because it is both interface dependent and thus limits the scope of the matrix manipulator's usefulness. The final memory has more uses than just in the context of a graphics display. One example is to perform these operations on a matrix of N-bit numbers; this requires stacking the modules N deep.

6.3.4 Algorithm Description

Figure 6.3.1 shows a block diagram of the sub-system that was implemented as a project. A square array of eight by eight one bit data cells is arranged in the center. The data cells are serially loaded with a bit map corresponding to the object to be read in a given orientation. Along the top of the array are a pair of shift registers which can propagate a *select* pulse along the top edge of the matrix in either the left or right direction. Each *select* line selects a vertical slice (column) of the bit matrix to be read. By propagating the select pulse from right to left or left to right, the columns of the array are read in their original orientation or their horizontal mirror image. The selected column is then loaded into a pair of shift registers at the bottom of the array which can also be shifted in both directions. These output shift registers are used to mirror the selected column about the horizontal axis. The serial output of these shift registers is the stored bit map in raster scan format.

As described, the hardware is capable of outputing the original matrix in any of its four mirror images. To obtain 90 degree rotations of these, an identical set of select and output hardware could be constructed along the horizontal axis. An alternative is to connect horizontal select line to the vertical ones along the diagonal of the matrix. In this way, the select and output logic is shared. Multiplexors on the inputs of the output register select either the vertically or horizontally selected words. Figure 6.3.2 illustrates the sequence of signals on the three control lines required to obtain a given orientation.

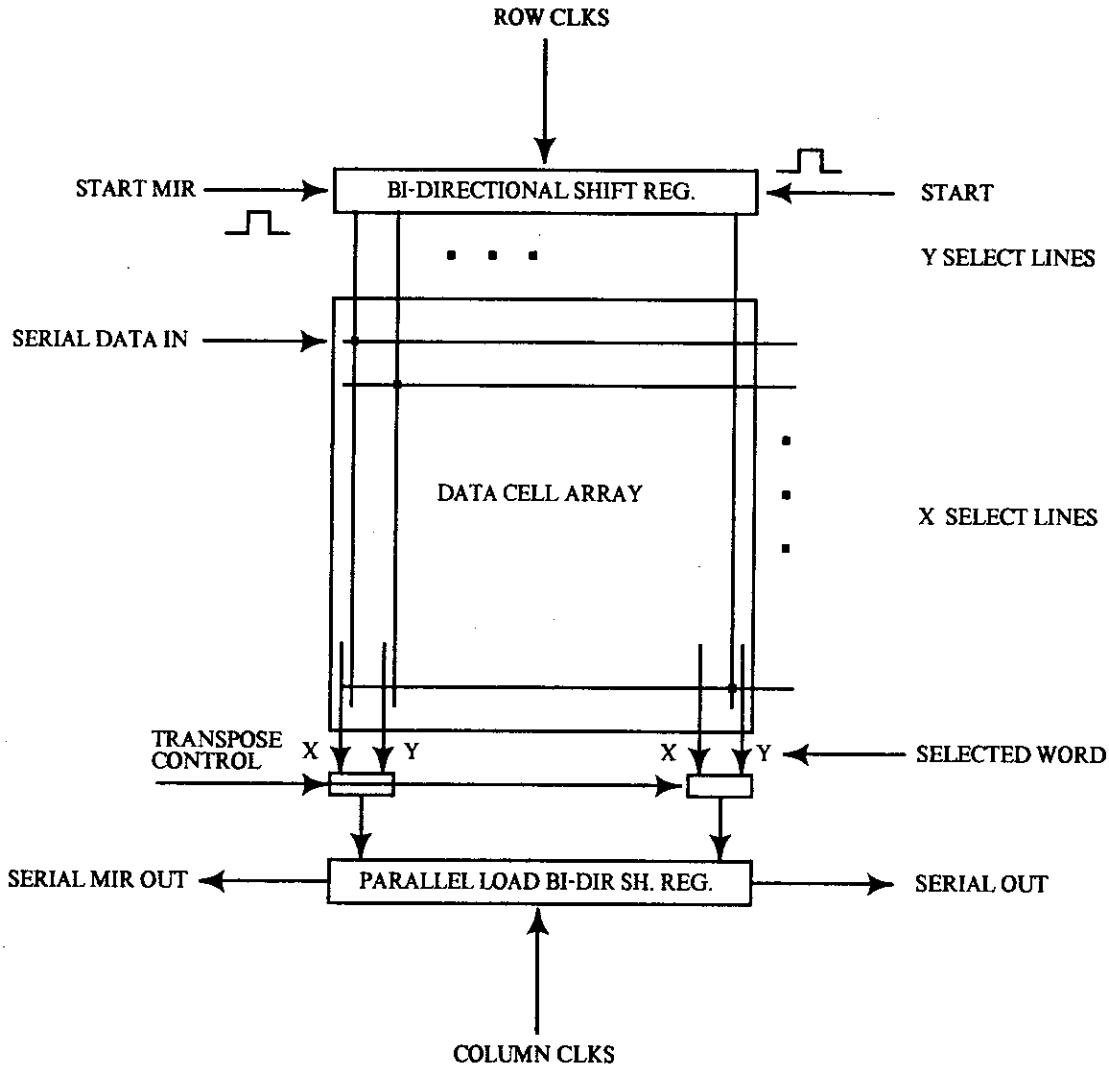

ROW CLKS
START MIR
BI-DIRECTIONAL SHIFT REG.
START
Y SELECT LINES
SERIAL DATA IN
DATA CELL ARRAY
X SELECT LINES
TRANSPOSE CONTROL
X
Y
X
Y
SELECTED WORD
SERIAL MIR OUT
PARALLEL LOAD BI-DIR SH. REG.
SERIAL OUT
COLUMN CLKS

Figure 6.3.1

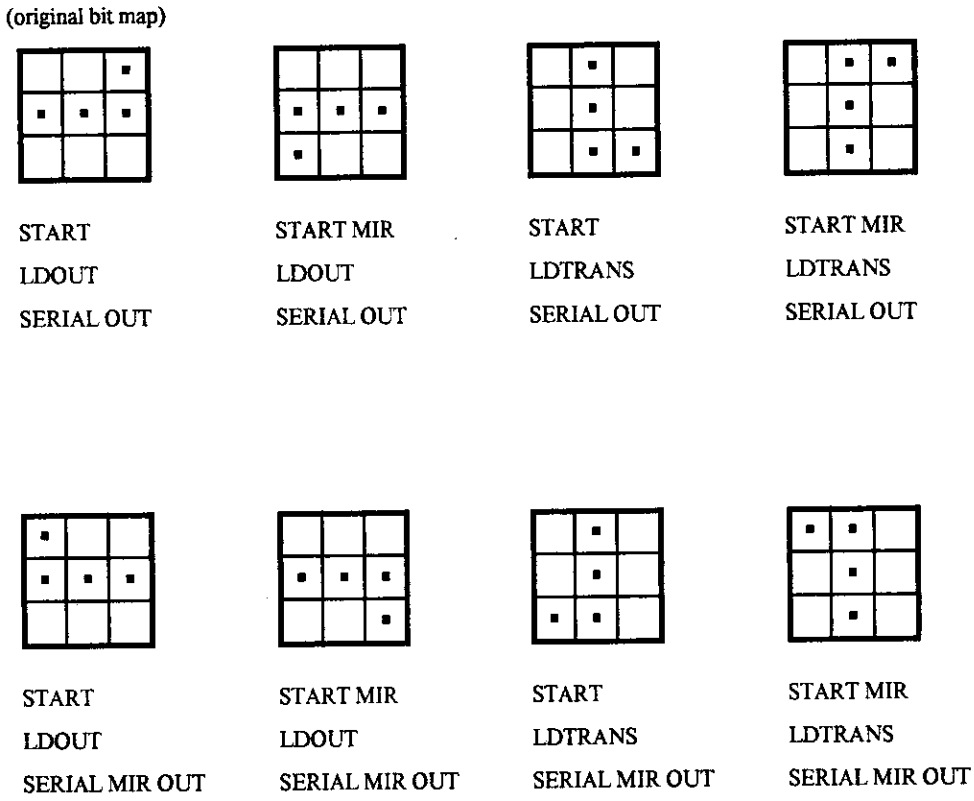
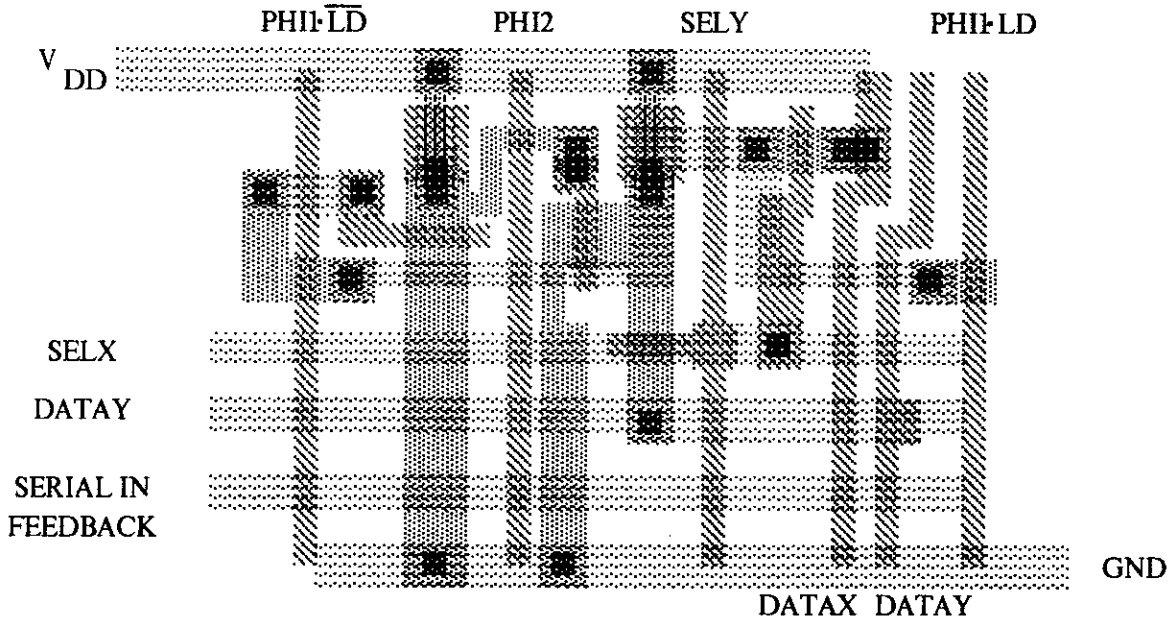


Figure 6.3.2 Available Transformations for a 3x3 bit matrix
Shown below each map are the control signals that are
asserted to obtain the indicated orientation.

6.3.5 Data Cell Design

Figure 6.3.3 illustrates the circuit used to realize the data cell. To minimize pinout, the entire array is loaded as a serial shift register by clocking $\varphi 1^*$LD and $\varphi 2$ while inputting the data on the DATA IN pin. The cell itself is simply a dynamic recirculating shift register. Clocks $\varphi 1^*\sim$LD and $\varphi 2$ run continously to refresh the cell. The select lines (X or Y) connect the output of the memory cell to an output bus orthogonal to the select line through a pass transistor. In order to have the DATAY buses come out at the bottom of the array, there are vertical DATAY lines also. Connections along the diagonal of the array map these horizontal buses to the vertical ones. In much the same way, SELECTX wires are connected along the diagonal to SELECTY wires. This means that a horizontal and vertical slice of the array are simultaineously selected. Both selected slices appear at the bottom of the array as eight pairs of DATAX, DATAY wires.



The circuit diagram corresponds to the topology of the layout. The array is loaded in a serpentine fashion, via a serial feedback wire that connects the last cell in a row to the first cell in the next row. This is also the same "raster scan format" of the original image. The serial output of the last data cell is connected to a test pad so that the loading of the data array can be tested independently of other functions.

The overall dimensions of a single cell are 45 by 70 square lambda. The cell is layed out such that V_{DD} and ground buses may be shared by mirror imaging alternate rows of the data cell array in order to conserve silicon area.

Since exactly one inverter in each cell is on at a time, the static power dissipation is:

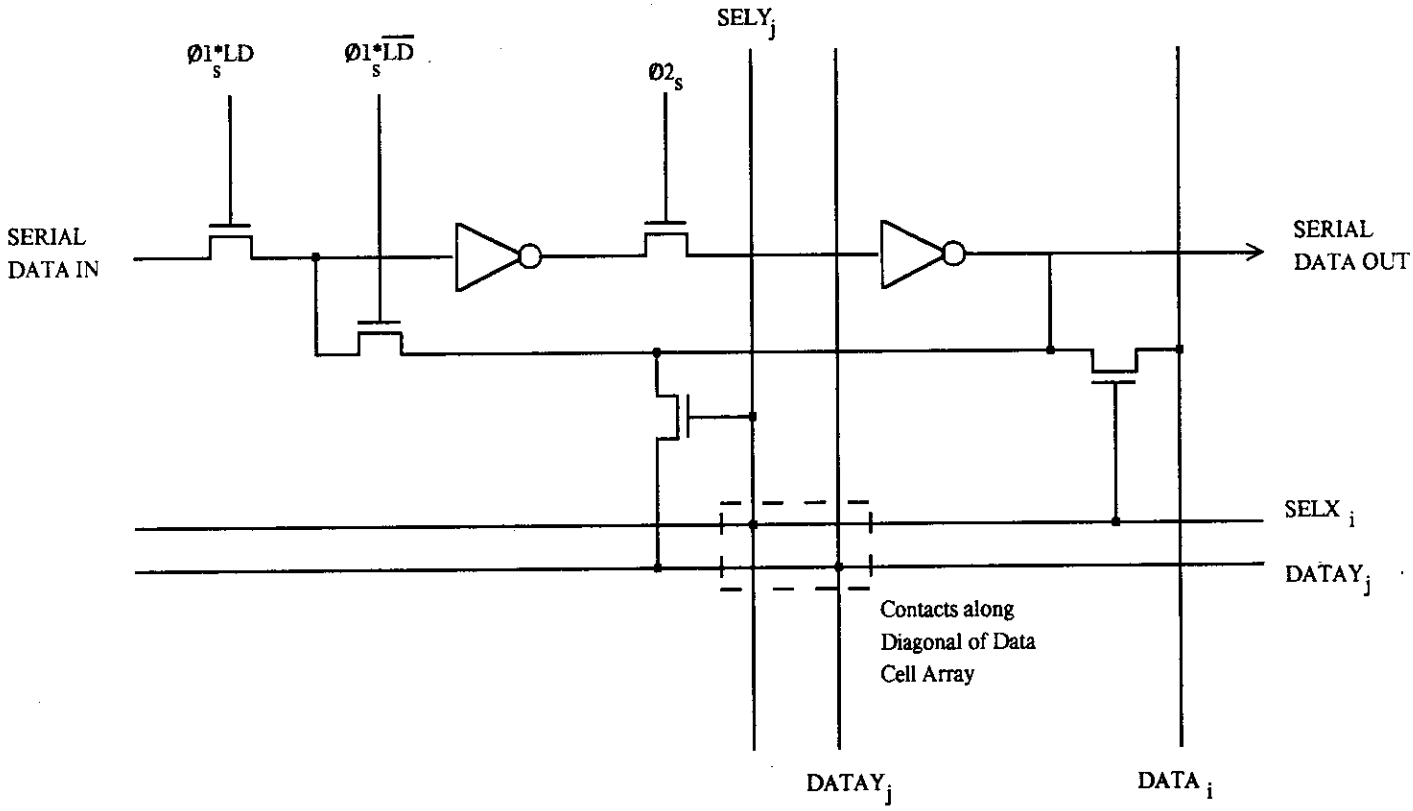


Figure 6.3.3 Data Cell Schematic

$$R = (1/3 + 3)\square * 10K\Omega/\square = 33K\Omega$$
$$I = V/R = 5v / 33K\Omega = .15\ mA$$

Thus, the entire array should consume about 10 mA.

A V_{DD} or Gnd bus wire must be capable of driving 16 cells, or 2.4 mA since it is shared by two rows. Assuming a maximum current density of 1 mA/μm^2, and 1 μm thick metal lines, the power buses should be capable of carrying:

$$4\lambda * 3\mu m/\lambda * 1\mu m * 1ma/\mu m^2 = 12\ mA$$

This indicates that the internal power buses are adequate. The internal power buses are connected along the vertical edges of the array with 10 λ wide wires which are in turn connected to power and ground pads at opposite corners of the array.

For a raster with 128 bits per line, the output shift register must be capable of shifting pixels out at a rate of 2 MHz. Row or column accesses of the array occur only one eighth as fast (for TV line rate). This means there is 4 μsec between row/column accesses.

For the data cell to be fast enough the output inverter pull-up transistors must source enough current to drive the relatively large capacitance of the DATAX and DATAY lines. The data cells on the diagonal of the array drive the most capacitance since they will be selected by both SELX and SELY lines and must drive both the DATAX and DATAY lines. Note that the DATAY lines consist of both a horizontal metal line and a vertical poly line. The total capacitance of these wires is:

$$C_l = 8[(3*70+27)*2.7*10^{-4}pf/\lambda^2 + ((2*48+8)+(2*35+3*12))*3.6*10^{-4}pf/\lambda^2]$$

$$= 1.1\ pf$$

The worst case for driving this capacitance is a low to high transistion. Refering to Chapter 2, page 17 of [Mead & Conway 1980] for the delay involved, we have

$$t = k\tau C_l/C_g$$

$$= 8 * 1ns * 1.1pf * 12*3.6*10^{-4}pf/\lambda^2$$

$$= 200ns$$

This is more than adequate for 128 pixels/line.

6.3.6 Select Register Design

The schematic of the select register is shown in figure 6.3.4. It consists of two shift registers which shift in opposite directions. The outputs at each stage are ORed together so that a pulse

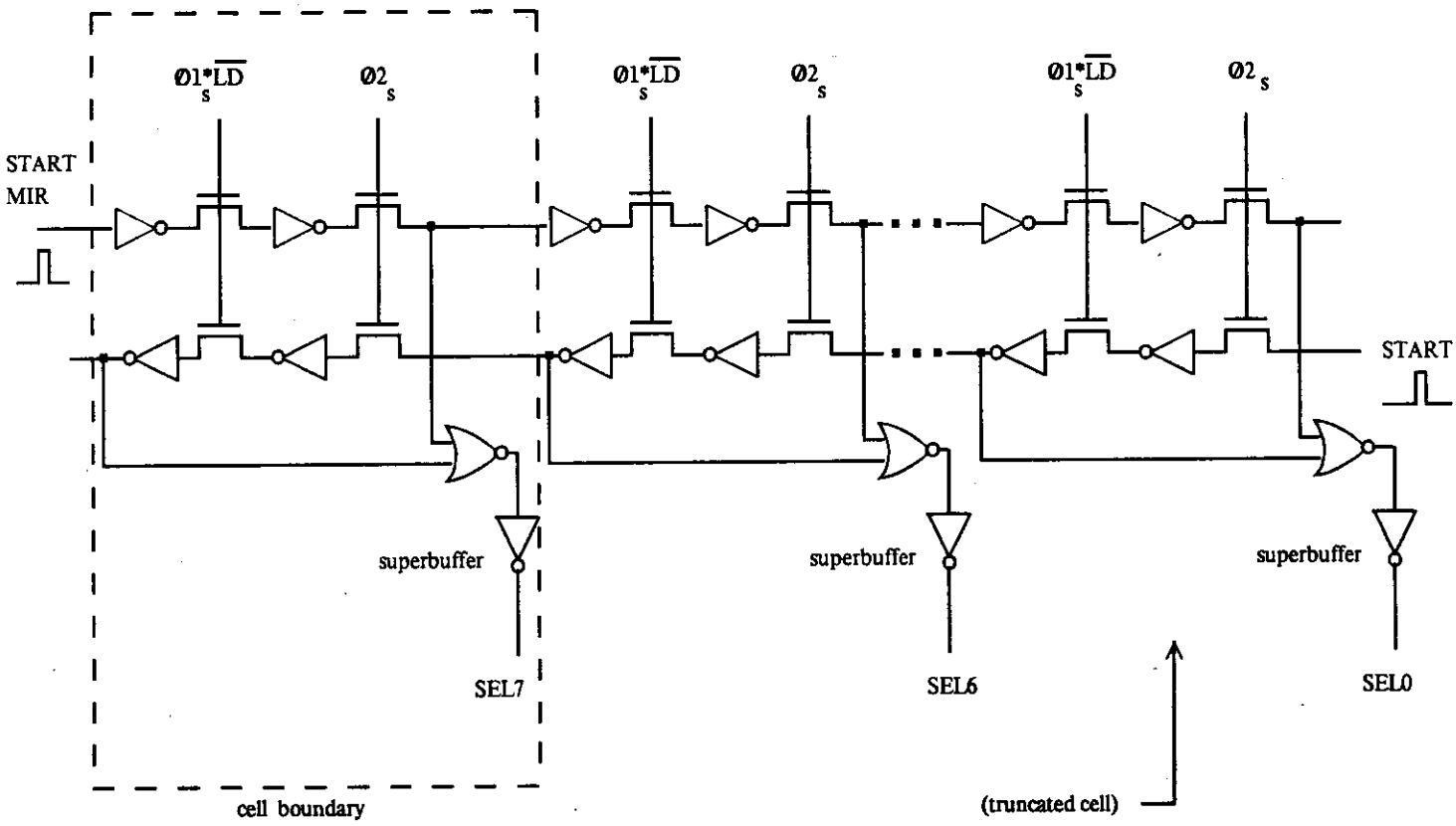


Figure 6.3.4 Select Register Schematic

propagating in either direction turns on the corresponding select line. The select lines are driven by super-buffers for speed. The output of both the top and bottom shift registers as well as SELY of each cell have large metal areas for wafer probing.

To initiate a read sequence the START or START MIR input is held high for one $\varphi 1$*LD, $\varphi 2$, clock cycle. This pulse then propagates through the select register . The same clocks that refresh the data cells are used to drive the select registers, since there is no harm in running them without a propagating start pulse. Figure 6.3.5 shows the layout of the basic select register cell. Bus lines to connect the various signals to the cells are included, to simplify the interconnect to the pads.

Each select register must drive a vertical poly and horizontal metal select line, plus their associated 16 pass transistors. The total capacitance of a select wire is:

$$C_l = 8[\ (45*2+16+16*4+14)*3.6*10^{-4}pf/\lambda^2 + 2*8*3.6*10^{-4}pf/\lambda^2 + (3*70+10)*2.7*10^{-4}pf/\lambda^2\ ]$$
$$= 1.46pf$$

This is driven by a super-buffer with the same size transistors as in the data cells, so that the time constant will be given by

$$RC = \tau C_l/C_g$$
$$= 1ns * 1.46pf / .043pf$$
$$= 33ns$$

since the rising and falling edges of the super-buffer's output will be symmetrical.

6.3.7 Output Register Design

The output register schematic is shown in figure 6.3.6. It consists of two parallel loading shift registers that run in opposite directions. A multiplexor at the top of the cell controls whether the original or 90 degree rotated image is output. Two outputs, one on the right, and one on the left of the output register are generated. Selecting which of these is used to drive the display provides mirroring control over the row/column of the array that is selected by the select register.

The clock lines that drive the output register are distinct from those that run the select register, since they must shift out an eight bit row/column for every row/column selected. These clocks are designated with an f subscript to denote "fast". Refering to the layout of this cell in figure 6.3.7, the gate of the pulldown transistor in top leftmost inverter, and the bottom right most transistor are omitted. This means that a logic 0 will be shifted out of the output register when no data is in it. This allows the output clocks to run continously to simplify the clock circuitry that drives them.

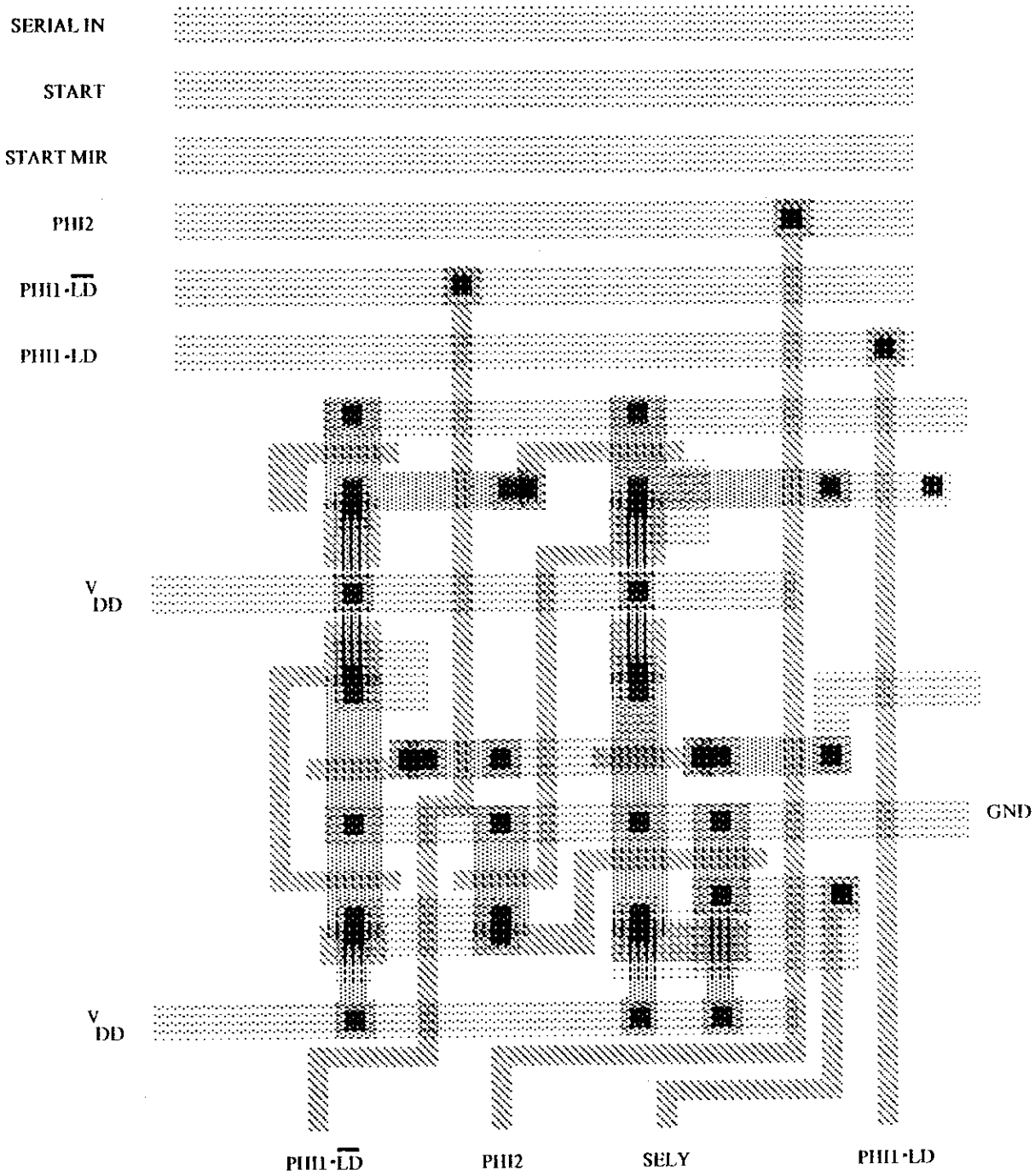


Figure 6.3.5 Select Register Layout

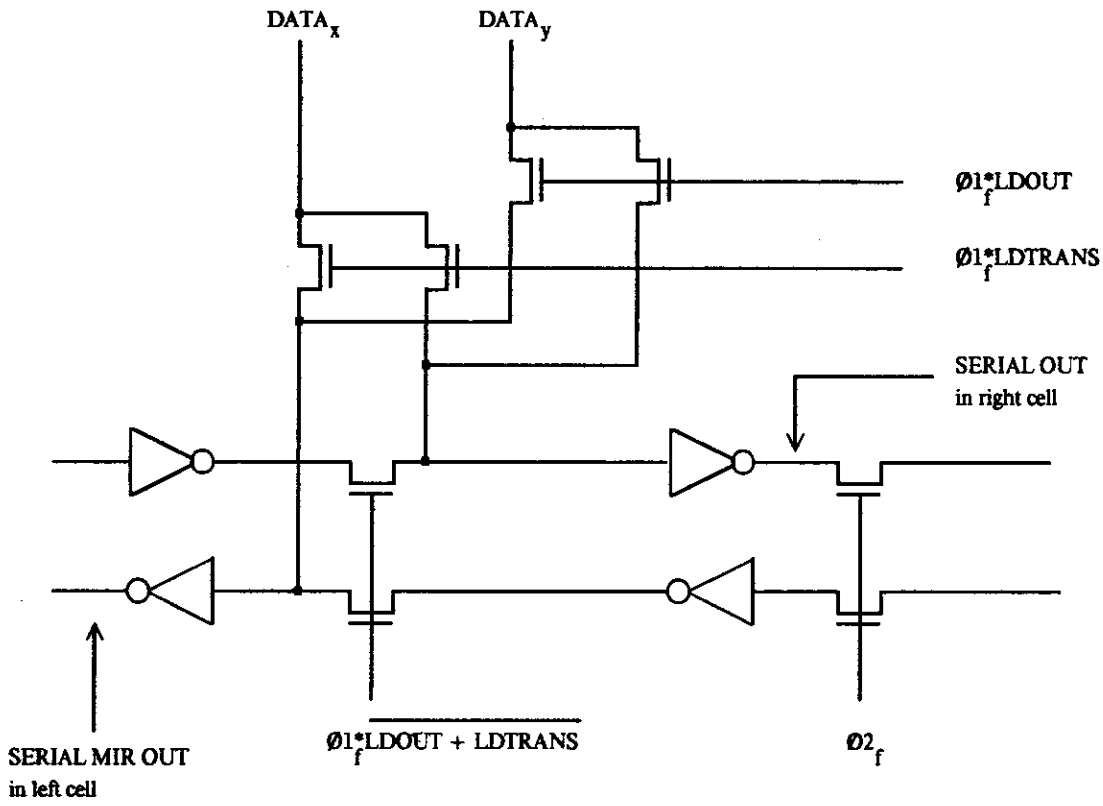


Figure 6.3.6 Output Register Cell Schematic

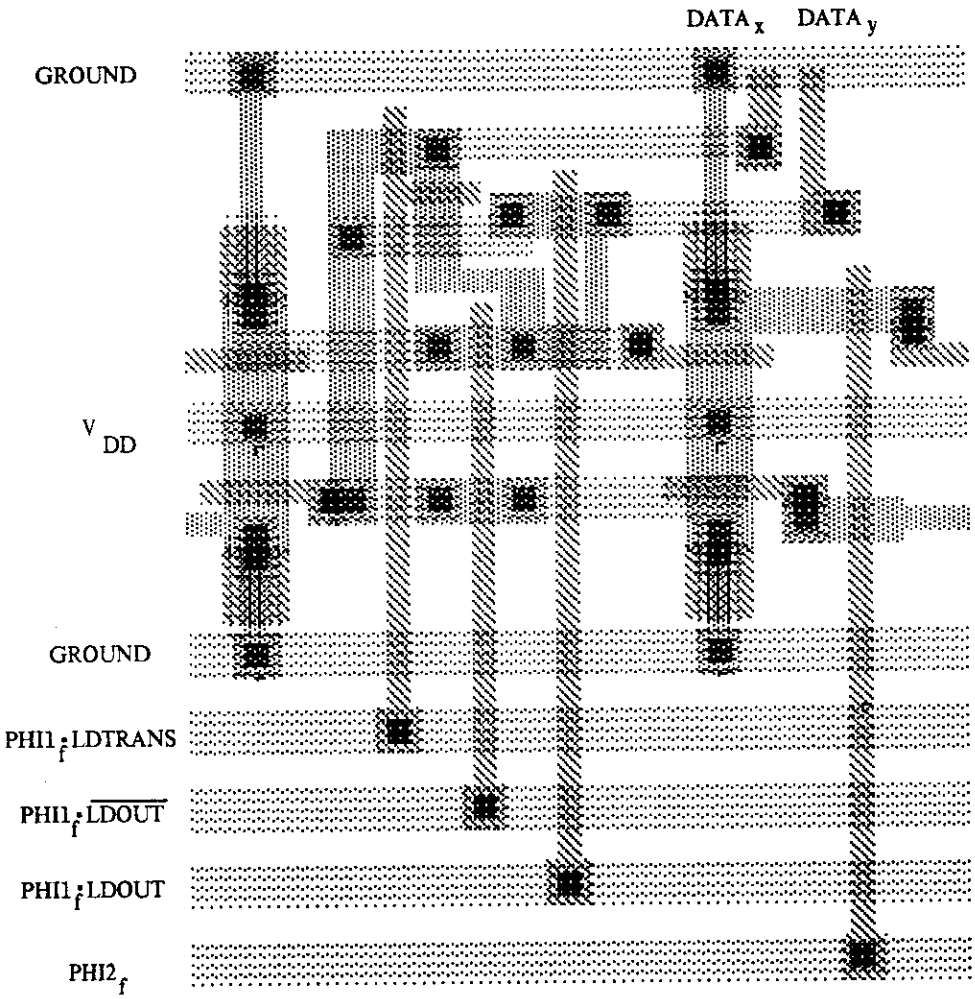


Figure 6.3.7 Output Register Cell Layout

6.3.8 Overall Timing

Figure 6.3.8 illustrates the timing of the various clocks. If the module is used in the graphics context described above, the slow clocks may be a two phase version of the horizontal sync pulse found in a raster type display. This occurs every 62.5 microseconds (for a 2MHz output bit rate), which is fast enough to keep the array cells refreshed. When external comparator logic determines that the first line of the object is being scanned, START or START MIR is held high. Similarly, a counter running at the pixel rate of the horizontal scan is compared to the X coordinate of the object, routing a $\varphi 1^*$~LD pulse to either $\varphi 1_f^*$LD or $\varphi 1_f^*$LDTRANS. Note that only equality must be detected (as opposed to "in region"), the clocks run continously, and do not require circuitry that counts out exactly eight clock cycles.

6.3.9 Testing

To test the fabricated chip, twelve TTL packages were assembled on a protoboard to generate all the necessary timing signals. Two 3-bit resistor ladder D/A converters were used to generate an 8x8-bit raster on an oscilloscope for displaying the image generated by the project. The Z-axis input of the oscilloscope was used to modulate the intensity of the displayed points.

Of the three bonded chips tested, two were 100% functional. Power consumption was 12 ma, as predicted. The project was also tested with the output shift register running at 2 MHz to test compatability with a 2 MHz CRT raster display system. At this speed the oscilloscope raster display was not functional so that the logic level of the output shift register was examined to determine if the transformations were correct. The two functional chips were successfully operated at this speed.

6.3.10 Conclusion

As is normally the case, this project was constraint by the limited time available and limits on the silicon area reserved for this chip. An obvious feature to add to this chip is the coordinate detection logic. This would not be to hard to implement, and would reduce the number of pins required.

References

[Dennard 1974]
R. H. Dennard et al, "Design of Ion-Implanted MOSFETS with Very Small Physical Dimensions," *IEEE J. Solid-State Circuits*, SC-9, October 1974.

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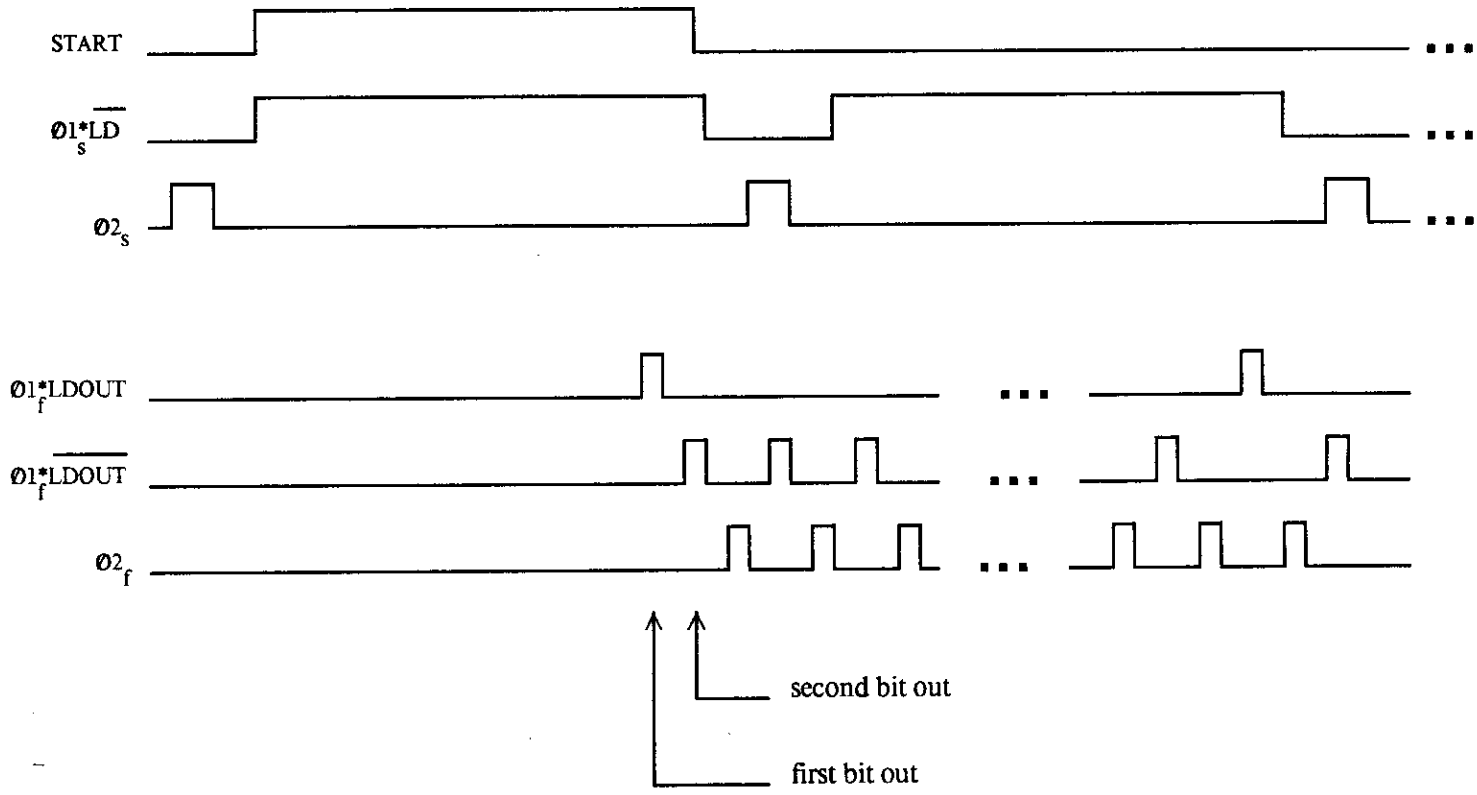

Figure 6.3.8 Timing Diagram for Readout Sequence

[Mead & Conway 1980]
C. A. Mead and L. A. Conway, *Introduction to VLSI Systems*, Addison-Wesley, Reading, MA., 1980.

[Wang 1978]
P. P. Wang, "Device Characteristics of Short-Channel and Narrow-Width MOSFET'S, *IEEE Trans. on Electron Devices*, ED-25, July 1978, pp.779-786.

For additional example projects see:

[Clark 1980]
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M. Foster and H. T. Kung, "Design of Special-Purpose VLSI Chips: Example and Opinions", Carnegie-Mellon C.S. Tech. Report, September 1979.