5. Mask Specification

When the chip has been laid out it must be converted into a format suitable for the pattern generator used by the mask house. This involves converting all of the shapes in the design file into rectangles and sorting them. The sorting order depends on the pattern generator; a penalty is paid in terms of the amount of time it takes to flash the reticle if the rectangles are out of order. Unfortunately the optimum order is based on a complex function which depends on mechanical considerations as well as the pattern being flashed; in general this function is not known to the designer. The moral is that unless the designer has detailed knowledge about the PG machine being used he is probably better off using a simple sorting algorithm (for instance lexicographic ordering based on what the particular PG machine is fastest at) than trying to second guess the pattern generator.

Before the PG tape can be sent off to the mask house some information must be obtained from the fabrication line regarding their process. The designer must tell the mask house the *polarity* of the working plates -- whether the plates for each layer should be *opaque field* (clear features) or *clear field* (opaque features). Typically a fab line will require a mixture of opaque and clear field plates, depending on the process step and the type of photoresist. The linewidths required by the process influence the choice of resist. More important, however, is the field area involved with the particular working plate. A speck of dust on an otherwise clear area of the working plate will cause a pattern to be made in the photoresist. If negative resist is being used the speck will make a hole in the resist which will enlarge somewhat due to undercutting in the subsequent etching process. Positive resist will leave a small dot where the speck was; this dot will probably be etched into oblivion. The fabrication line decides which of these factors to trade off in choosing the polarity of the working plates.

Varying etch conditions may cause the fab line to request that features on the masks for certain layers be altered by a constant amount (e.g. 0.5 micron around any border) in order to produce the desired dimensions on the silicon. The dimensional adjustments can be made in one of three ways:

> The circuit designer can be required to change his design to take into account the over- or under-etching at the fabrication line. This probably entails considerable work on the part of the designer each time the circuit is implemented on a different fab line, but has the advantage that the designer retains complete control of the layout geometry.
>
> Software could be provided to input the original design file and produce a new design file

which had the borders of features expanded or contracted in the appropriate way. This approach may require the use of complex algorithms in order to correctly modify the original file since minimum spacing design rules may be violated by enlarging adjacent features while gaps and discontinuities may be introduced by shrinking features which abut in the original design.

The mask house may be able to effect the changes by adjusting exposure time and other parameters in the mask generation process. This produces satisfactory results if the expansion or contraction is within the range attainable by the mask house.

In general it's a good practice to identify which layer each mask belongs to; the fabrication line may have specific codes that they wish placed on the masks for identification purposes.

Once all of this information has been collected and reduced to a PG tape and some written instructions the mask house takes over. When the working plates are returned they are passed in turn to the fabrication line along with more instructions. The total elapsed time for mask making and wafer fabrication can be 8-12 weeks. During this time the designer should be preparing for the day when the wafers are finished.