1. The New IC Designer

Traditionally the design and development of integrated circuits (IC's) has been the domain of specialists with substantial training in this "art". With the emergence of more powerful computer aids and of reasonably standardized IC processing techniques, IC design can be simplified to the point where it becomes a routine engineering step in the development of a special purpose system. MOS devices are particularly simple and straightforward as long as one stays away from the smallest geometries feasible. With reasonable, relaxed design rules the performance of standard MOS circuit blocks such as inverters, pass gates, buffers, NOR gates and composites of these blocks become as predictable as TTL circuits. Using a structured design approach, such as the one promoted by Mead and Conway in *Introduction to VLSI Systems* [Mead 1978], it is possible for people with only a minimal understanding of the device physics of a MOS transistor to produce operational integrated circuits of substantial size. Thus, a systems designer can now sit in front of an interactive graphics terminal and produce the layouts of a set of masks for a special purpose integrated circuit. Such personalized IC's can greatly enhance the functionality of the system to be built or alternatively may dramatically reduce the total chip count for a system of given specifications.

In such a venture it is often not important to produce an integrated circuit of the highest layout density or of the highest performance, which could only be obtained by pushing the limits of present-day technology. Normally the main concern is to get a properly working chip with the shortest possible turnaround time. It is here that effective design tools and, even more importantly, the proper design methodology, are crucial. These issues are discussed in *Introduction to VLSI Systems*. The second, equally important part is to get the IC designs implemented. In an environment that is not already set up to produce custom-designed IC's as a routine step, the designer himself often has to be the driving force behind the implementation of the first few IC's. In this situation many months are often wasted because of unsuitable preparation or unavailability of the necessary information, leading to frustrating delays in the project schedules and to abandoning the custom-made IC approach altogether. These are problems that we hope this document will prevent.

Converting an integrated circuit design into a finished, packaged, and tested chip is more a time consuming task than a difficult one. Dozens of important details have to be observed to prevent disasters or costly delays. Up to this point a concise description of the specific details and necessary steps has not been available. Specific information had to be gathered from scattered sources including personal interviews with "old hands in the trade".

This document is intended to be a guide along the entire path from the design of the layout of the integrated circuit, through mask generation, IC wafer fabrication, and chip packaging to the testing of the finished circuits. Important decision points and potential pitfalls along the way are clearly spelled out.

Often several IC designs will be combined into a single multi-project chip. In this manner the cost of mask generation and wafer fabrication, as well as the organizational overhead involved in pushing the future IC through all critical stages can be shared among a larger group of people. In an academic or research environment this coordination of several experiments into one IC project is particularly important, so that not every student has to worry about all of the details of mask and wafer processing. Certain features such as test patterns to measure device performance, alignment marks, and chip separation lines (scribe lines) can be standardized and re-used in subsequent multi-project chips. Sticking to the same features, similar basic chip formats and established procedures to generate the multi-project chips will help to streamline this process and enhance the chance for satisfactory results. Someone, therefore, will have to act as a coordinator. His or her first task will be to merge the different files describing the various IC designs with the starting frame containing the mentioned standard features. He will then interact with the mask house and the fabrication line, making sure that both places have all the information that they need and that there is no misunderstanding in what they are expected to do. In order to avoid unnecessary delays he should constantly keep track of the state of the project and try to effect smooth interactions between the various parties involved. This includes hand-carrying the magnetic tape with the designs from the research site to the mask house, the set of working plates from the mask house to the fabrication line, finished wafers from the fab line to the dicing and bonding station, and finally a number of packaged chips to the testing area. This document describes the real-life problems and details which the coordinator must be aware of to effectively carry out these tasks. But even the occasional designer of an individual IC should be aware of the overall process, so that he or she may better understand certain implications on their own activity. As with any other system implementation technology, the types of design aids and the methods of fabrication impact the type and quality of design which is done. The most effective systems designers will therefore understand at least the basic aspects of design aids and checking tools as well as mask and wafer fabrication.

Chapters 2 through 6 outline the basic path from IC design to the finished product. Chapters 2, 3 and 6 should be studied even by people who never dream of becoming coordinators of multi-project chips, since they set the stage for proper IC design. For the coordinator chapters 4 and 5

are absolutely vital. Chapter 7 gives an example of a multi-project chip produced at Xerox PARC during the summer of 1978. It carried 10 experiments including a wide range of logic, arithmetic and memory circuits and a test pattern. Appendix A contains a listing of the instructions sent to the mask house concerning this particular chip.

Throughout the text *italics* are used to introduce vocabulary which the designer should know. No attempt is made to tabulate precise definitions of terms, but enough information can be inferred from the context that the reader can search for more details if necessary. Appendix F provides pointers to in-depth articles and texts covering particular aspects of IC implementation. Integrated circuit manufacturers can often provide valuable information and insight into most phases of IC implementation; Appendix B is a listing of some that we have dealt with. It is by no means exhaustive, and the reader should not hesitate to make his own contacts where possible.