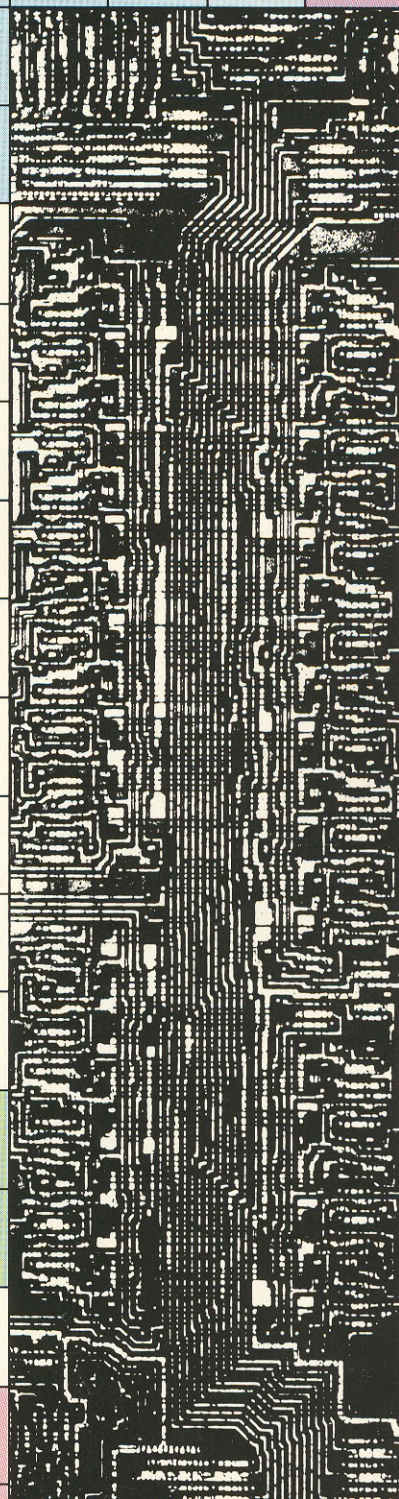


INTEGRATION

the VLSI journal

Volume 1 Number 1 April 1983
ISSN 0167-9260 IVJODL 1(1) 1-104

North-Holland



INTEGRATION

L. SPAANENBURG
 Dept. of Electronic Engineering
 Twente University of Technology
 P.O. box 217
 7500 AE Enschede
 The Netherlands

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Aims and Scope

INTEGRATION'S aim is to act as a professional journal on a quarterly basis covering every aspect of the VLSI design and testing field. Technical, commercial, legal, social, educational and managerial aspects of the business will be covered, with the technical aspect normally predominating. The journal is distinguished from others by its coverage of all relevant subjects ranging from new architectures and integrated design systems to standard process technologies, functions and test configurations. Individual issues will feature tutorials and articles giving information on the status of new methodologies and standards. Furthermore special niches will be devoted to the presentation of standard (or generalized) design interfaces with process technologies, to reuseable functions laid out in these processes and to test devices ('canaries') and schemes.

Range of Topics

The following provides a listing of the types of subjects which will be covered:

- Integrated CAD systems/data structure, description language, hardware requirements, data base management
- Design courses: concept, methodology, multi-project chip
- VLSI architecture of microprocessor, signal processor, interface, dedicated system etc.
- Tools: algorithm, programming language, description standard, stand-alone design system, ergonomics, graphics
- VLSI algorithms, complexity theory, performance area relation, wiring model, reliability
- Process-technology: generalized process-description, design constraints, technology-independency
- Testing: test procedure, design for testability, test system architecture
- Market survey: brokery, legal aspects, economy, customer/manufacturer interface
- Design concepts: silicon compiler, chip assembler, use of higher-level programming languages
- Mathematical Foundations: algorithms, procedures, notations, NP-completeness

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The northern route

You may wonder whether the NORDIC countries are really part of Europe; you may never wonder whether they are part of the VLSI community. They did not do the usual thing in creating national development programs. Instead they collaborated in the NORchip project. Designs, aimed for a CMOS process-technology, were merged at Linköping University and at Sentralinstituttet for Industrial Forskning in Oslo. From there they were sent to European mask generation, wafer processing and bonding sites.

The first NORchip contained 15 designs from 10 institutions and was collected at February 15, 1982. A second run occurred in June with 2 more to follow. Details will appear in a forthcoming issue of INTEGRATION, *the VLSI journal*.

Sources

- NORchip, The NORDIC countries on one chip, 1982.
 - Svensson, C. and R. Sundblad, A CMOS design manual, Rept. LiTH-IFM-IS-72, Linköping Univ., 1982.
-

Australia steps into the silicon age

A remarkable addition to the list of nations, that have entered the silicon age, is Australia. Here it was recognized, that you cannot compete with the years long experience of well-established semiconductor factories. As in the beginning there was nothing in this line, one had to seek for alternatives. So the separation between design and fabrication, as pioneered by Professor *Carver Mead* of the California Institute of Technology and Dr. *Lynn Conway* of Xerox Research in California, was warmly wellcomed. Under the guidance of Dr. *J. Craig Mudge* (Fig. 1), who returned to Australia after living at the U.S. frontier line for years to

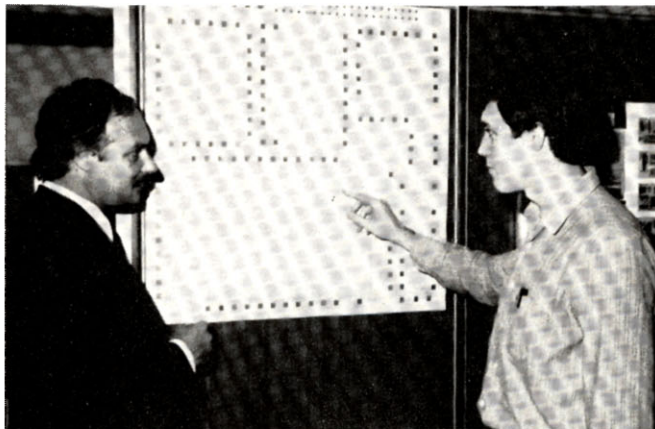


Fig. 1. Dr. *J. Craig Mudge* (left), head of CSIRO's VLSI program and Mr. *Robert Clarke*, who coordinated the first Multi-project Chip Implementation System.

head the VLSI program of the Commonwealth Scientific and Industrial Research Organization (CSIRO), a Multi-project Chip Implementation System was created. *Mudge* also gave a crash course on VLSI. His attendants also gave courses and so

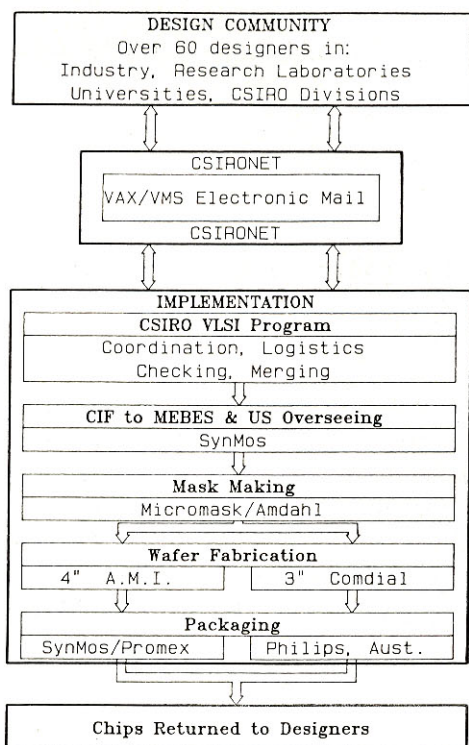


Fig. 2. Overview of the AUSchip implementation procedure.

on. From this pool of designers emerged at the end of May 1982 the first Australian MPC, coordinated by Mr. *Robert Clark*. It contained 46 different designs from 21 predominantly Australian institutions.

Until May 31 the designs were taken in at CSIRO, checked for design rule consistency and merged into five chip types. The maskpattern tape was sent to the United States of North-America, where both mask making and wafer processing took place, packaging in turn being done in Australia. A complete breakdown of the AUSchip procedure is given in Fig. 2. This MPC run was a great success, soon to be followed by a second run at November 30, 1982, and a third one is currently under way.

Sharing silicon is not a unique enterprise, but what makes the AUSchip especially worth noting, is that it shows how VLSI brings people together on a

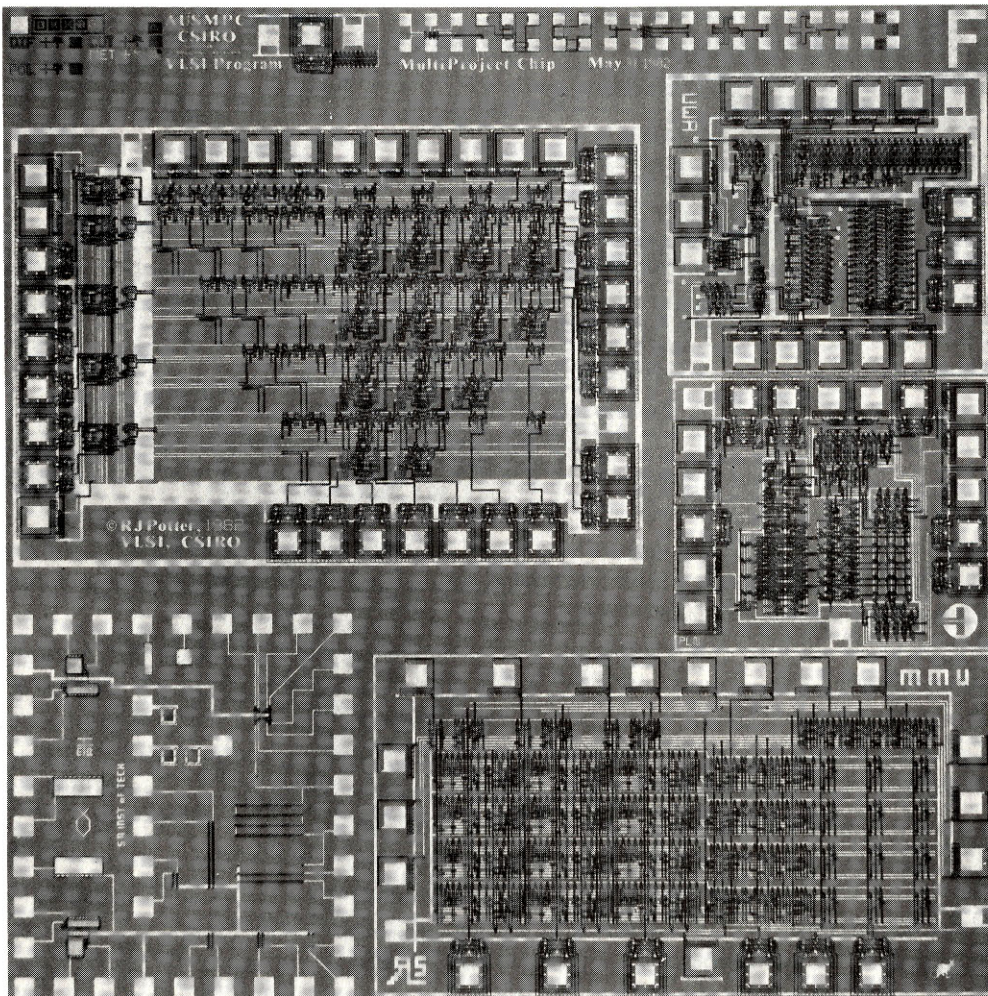


Fig. 3. Microphotograph of project F with the dutch inclusion (an associative memory management unit) in the lower right corner.

world-wide basis. On the May '82 MPC one of the designs originates from Twente University in the Netherlands (Fig. 3). Quite the opposite part of the world! Then on the November '82 MPC there were 2 US designs included, and who knows which foreigner will be present on the third chip set.

Sources

- CSIRO Industrial News, nr. 154, September 1982.
- Clark, R.J., AUSMPC 5/82 designer documentation, August 1982.

VLSI teaching at DIGITAL

When the Mead and Conway train began to move in 1979, DIGITAL was one of the first to get on board. They did so in a rather peculiar way using outside university help. *George Williams* of Union College and *Lance Glasser* of MIT were sponsored to take the summer '79 course that took place in Washington. On return to Hudson (MA) they taught a DIGITAL internal Introductory Course on Structured MOS Design. A student chip design project was attempted, but few design aids being available only two designs were really completed.

From this sprout a little tree has grown. The enthusiasm of many people with among them *Lee Williams*, *Del Thorndike* and *Alain Hannover* brought about a smoothly running well-equipped sequence of 8 courses. Among them is still an improved Introductory Course, wherein 2 hired university staff members rush a maximum of 40 attendants through VLSI in 10 days. Being held for four times a year it has created a better understanding throughout the company for the basic needs of this high-technology.

At most 10 happy few engineers can proceed to the Student Chip Design Project Course. This course is run 2 times a year tutored by 3 hired university staff members and takes a minimum 10 weeks period. The number of design aids has grown respectably over the years and cover by now amongst others system architecture, logic simulation, logic synthesis, circuit simulation, mask layout design, design rule check and circuit extraction.

The success of the courses can be viewed by looking at DIGITALS most recent professional designs. This indicates, that the teaching environment has gradually evolved to a prototype workbench (Fig. 4). In other words, the Mead and Conway style has left the schoolbenches. It is not just a course anymore. Details of the DIGITAL endeavour will appear in a forthcoming issue of INTEGRATION, *the VLSI journal*.

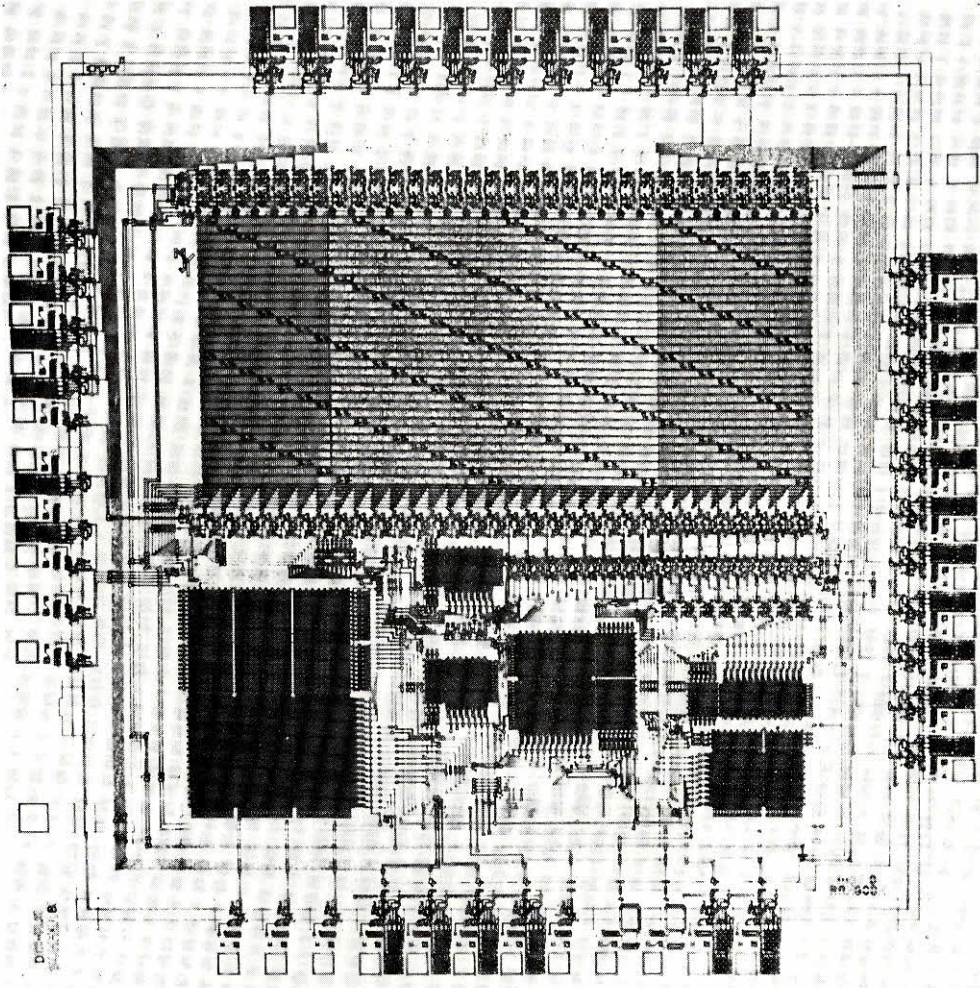


Fig. 4. An instruction buffer as produced on the DIGITAL student design workbench.

Sources

- VLSI student chip projects, Graduation manual, December 1981.
 - Williams, L., Technical education for engineers at Digital Equipment Corporation: A report of two years into a program in LSI, Februari 1982.
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