

III. FUNDING THE FACTORS

Having orthogonalized those factors that lead to improvements in semiconductor circuitry, we can now identify the major efforts currently underway and recommend support for activities not adequately covered. In the following discussion, we will elaborate on the four recommendations summarized in Table 1 regarding the efforts that should be directed toward factors 1, 4, 5, and 6 in that table. We believe that the existing private funding is not and will not be adequate to accomplish the work that needs to be done in these areas.

FEATURE SIZE (FACTOR 1)

Our first recommendation is that the limits of feature size (factor 1) permitted by semiconductor physics be explored. There is much to be learned about the fabrication processes, defect mechanisms, and performance of such small devices, independent of the difficulties introduced by making complex chips. It may be, for example, that a whole new set of defect mechanisms exists for very small devices that would cause us to alter, dramatically, our expectations of chip yield. Then there is the possibility that devices with 0.1-micron features may prove sufficiently faster than larger devices to warrant their production even in simple circuits. Finally, simple techniques for making very small devices may be found that capitalize on the small size and are not applicable to larger devices. It is certain that experience with very small devices will serve to verify theoretical predictions, and experience in making them will provide valuable insights into the course that our minification efforts should take. For example, subthreshold currents become larger as size is decreased and probably will make dynamic devices with very small features unusable at room temperature.

Early experience with small circuits helps us to avoid two difficulties that could be encountered with a continuing gradual decrease in feature size. Very small circuits will require voltage levels much lower than those now in use. With some agreement on what these ultimate standards might be, we may be able to avoid a series of standards

changes. As will be shown later in this report, in order to make very small circuits with electron beams, it will be necessary to use electron-sensitive "resists" similar to those now available; resists that are more sensitive to electron radiation are relevant only to devices with intermediate-size features. Experience in the manufacture of very small circuits may obviate the need for developing more sensitive resists. It is possible that from efforts aimed at making small devices, albeit in small numbers, there will emerge a complexity at the new size scale that will leapfrog the combined efforts to decrease size and increase complexity now prevalent in industry.

Devices with very small features are more important for defense applications than for commercial exploitation. In many defense applications, size, weight, and power-consumption limitations are severe, so that very small devices are essential. Also, very small devices have the potential of providing an enormous amount of compute power, not only because of the numbers of them that might be interconnected but also because of their high speed. This power will be vital to a number of signal-processing applications important to defense needs. Moreover, privately funded efforts are not trying to develop devices as small as are theoretically possible because of their economic need to maintain complexity and their inability to bear an additional development burden. If new developments are to result in very-small-size devices, new funding will be required.

CHIP SIZE (FACTOR 2)

There is adequate private investment for improving chip size (factor 2). The economic reasons for increasing chip size are so obvious that every semiconductor house in the country is continually trying to improve yields and thus make larger and larger chip areas available. Theoretical efforts aimed at gaining a fundamental understanding of the ingredients that affect yield are already in progress under ARPA sponsorship at the University of Florida. There seems to be no justification for recommending additional research efforts in this area.

COMPONENT COUNT (FACTOR 3)

The benefits of improving component count (factor 3) are readily apparent, and the semiconductor industry is already considerably motivated by the competitive economics in this field. The relatively rapid development of commercial semiconductor memory technology, for example, is the direct result of improvements in component count and chip size.

REPLICATION PRECISION (FACTOR 4)

Our second recommendation is that research efforts be aimed at a better understanding of the fundamental limitations to replication precision (factor 4) imposed by the properties of semiconductor materials. Replication precision, as separate from feature size, chip size, etc., seems to be poorly understood by the industry. How much distortion is experienced by silicon as it is passed through the severe environments required for semiconductor processing is not well known, nor is there a clear understanding of the factors that influence these distortions. A program of research aimed at developing a basic understanding of these mechanisms would be invaluable in guiding the development of the industry. Although the beginnings of such efforts are evident at several industrial laboratories, the approach taken in each case is quite ad hoc, merely being aimed at solving the problem well enough to take care of the complexity of the replications now being contemplated. We believe that a solid national understanding of this problem will be valuable.

SYSTEM CAPABILITY (FACTOR 5)

Our third recommendation is for research leading to an understanding of the organizational factors that influence system capability (factor 5). While it is widely recognized that wiring dominates the cost of computing equipment today, there is little theory on which to base designs. The logic minimization theory that is available minimizes relay points or gates, not wires. The geometric and topological problems introduced by the need for wires to pass one another are formidable and present a major design obstacle to obtaining circuits

that implement complex logical functions. The traditional methods of organizing computing machines were developed in a technology in which the separation between memory and logical processing was clear, a separation no longer necessary or even desirable. Traditional design methods have treated logical functions and wiring geometry as independent of one another; this approach can be very costly in microcircuit technology where wiring dominates the cost of logic.

Organizational factors also influence our ability to make new designs easily. Traditional electronic packaging methods have served not only to house elementary electronic functions, but also as logical separations in the design process. The designer of a "component" packages that component not only physically by providing a housing for it, but also logically by providing a functional description that states its terminal behavior and shows typical applications. Integrated circuit technology has reached a level of complexity where such functional descriptions are often too complicated to be fully useful. In effect, by placing more and more logic on a single circuit chip we are eliminating the natural design separation points previously provided by the package. We will have to replace these points with arbitrarily chosen divisions of the logic design process for the integrated circuit itself. The division points will be much like those used in another homogeneous logical medium: software. We need to learn how to choose such divisions wisely so that the generality of the functions provided by a designer on one side of an arbitrary division point will be available to a designer using his design, but will not overwhelm him; such design interfaces need to be both simple and general.

The influence of organization on performance is in some sense an extension of the "device and circuit cleverness" ideas put forth by Gordon Moore (see Appendix B). According to Moore, much of the increase in component count achieved in the past decade has resulted from our growing cleverness in electronic circuit design and in fitting components together. He points out, however, that circuit and device cleverness is about exhausted as a source of improvement in component count. While this is undoubtedly true, we believe that compute power, not component count, is the proper measure of value. We maintain that

at a higher level of organization the same kinds of cleverness that resulted in higher component counts will enable us to get more compute power per component, particularly in systems in which there are many thousands of components and, more important, many thousands of wires.

The need for new organizations of information-processing equipment is overwhelming in almost all areas of defense. Literally tons of data go unprocessed each day because the means for processing them are inadequate. Machines able to interpret pictures, to search large data bases quickly for "interesting" coincidences, to extract signals from noise in radar, sonar, and other sensors, to perform target identification, and to model complex military and economic processes are invaluable to defense. Organizational innovations such as commingling computation and memory functions may serve to bring our computation capability much nearer to the as-yet-poorly-understood limits imposed by the size of our devices, their switching speed, and the speed of light.

We are recommending, therefore, that ARPA initiate a research program to determine how computing machines can best be organized, based on the implications of today's semiconductor technology. Such research should lead to the development of new kinds of organizations and new theories of organization that will meet the level of complexity demanded by future semiconductor devices.

WAFER SIZE (FACTOR 6)

Our fourth recommendation is for a research effort that will result in a better understanding of the optimum choice of feature size, chip size, and wafer size (factor 6), given the constraints of the newly emerging manufacturing technologies. We are concerned that the choices being made by industry in these areas are driven primarily by historical factors that may no longer be relevant. It will be very difficult, for example, to retreat from the 4-in. wafer. However, a careful examination of the choices now being made by industry may have a major effect on guiding the industrial developments in the next decade. Such a study would probably be a one-time effort, rather than a continuing project.