II. IMPROVEMENTS IN INTEGRATED CIRCUITRY

Improvements in integrated circuit technology can be separated into two basic types: improvements in the devices themselves, i.e., functional improvements such as the speed of a memory; and improvements in the cost of the devices, i.e., fabrication improvements such as projection wafer exposure. The effects of these improvements on six important factors are summarized in Table 1 and are described in the following paragraphs. It is essential to consider these effects separately. Because many of them seem to interact, there has been a widespread tendency to confuse their separate implications.

FUNCTIONAL IMPROVEMENTS

Integrated circuits have been improved by minification of their features. Reduction in the size of circuit features not only permits more circuitry per unit chip area, but also improves the speed of the devices, particularly for metal oxide semiconductor circuits (MOS). Reductions in size have usually been accompanied by increases in the number of circuit elements connected together or fabricated together. This has often led to confusion between minification and complexity, a confusion to be avoided here.

Another improvement that has been made is in the size of chips that can be manufactured with adequate yield. These improvements have impact on both function and fabrication, as we shall see shortly. Working circuit chips have steadily become larger over the years, providing more area in which to pack the components and bonding pads and more power-dissipation capability. Larger chips also increase the lengths of the longest wiring runs, introducing both time delays and the need for more careful electrical design to prevent excessive voltage drops. Improvements in the size of chips derive from improvements in the defect density of the materials used and in the number of defects introduced in pattern replication. Functionally, chip size is important because it permits more logic capability without the need for off-chip interconnections.

Table 1

FUNCTIONAL EFFECTS AND FABRICATION LIMITATIONS RESULTING FROM IMPROVEMENTS IN INTEGRATED CIRCUITRY

Factor	Functional Effects	Fabrication Limitations	Recommendations
1. *Feature Size:* Dimensions of circuit elements and spaces between them.	Smaller → faster; changes voltage and impedance levels.	Limited by fabrication process and/or alignment precision.	Explore the limits permitted by semiconductor physics.
2. *Chip Size:* Overall dimensions of a complete circuit.	Affects permissible power dissipation, number of bonding pads, and length of longest conductors.	Now limited by yield; relation to feature size unknown.	Industry will do it.
3. *Component Count:* Number of active devices on a chip.	Device and circuit improvements have made component count go up faster than accounted for by feature size and chip size alone.		Industry will do it.
4. *Replication Precision:* Relative stability of each element of a pattern to any other.		Limited by dimensional stability--sufficient for a whole wafer at present dimensions, i.e., 1 μm in 10 cm or 10^{-5}.	Understand the fundamental limitations imposed by anomalous deformation of semiconductor materials.
5. *System Capability or Functional Complexity:* Measure of compute power of a device.	For a given component count, compute power may be greatly improved by system design cleverness; for simple memory this has already been done.		Explore new organizations; understand fundamental limits imposed by wiring geometry, device performance, and speed of light.
6. *Wafer Size:* Size of substrate processed as a unit.		Was equal to replication size. Will become just a handling consideration.	Understand the optimum choice of *feature size*, *chip size*, and *wafer size* given the constraints of the submicron manufacturing technologies.

A third area of improvement is in circuits and devices. The component count available in integrated circuits has been increased over and above the level accounted for by the improvements in chip area and feature size. We have become more clever in making devices and circuits and in packing them together so as to get more devices per unit silicon area. According to Gordon Moore (see Appendix B) these improvements in component count have been more significant in the past decade than improvements in either feature size or chip area. Moore predicts, however, that this source of improvement is nearly exhausted.

Functional improvements have also been made in circuit organization and machine architecture. An integrated circuit is intended to perform a certain function and its user cares only that the function be performed faithfully and that the device be as inexpensive as possible. With circuits reaching component counts of over 10^4, and soon to reach from 10 to 100 times that number, it is not surprising that new ways of organizing circuits are being found that will function equally well with fewer components, or that will provide much more function per component. Even more important is the measure of logical function per unit circuit area, since in most circuits most of the space is taken up by wires rather than by components. As component count increases, more wires are required and these wires, on average, must be longer, so that more of the circuit area has to be devoted to wiring unless great care is taken in organization.

Historically, much of the progress in circuit organization has been made by using regular implementations to implement complex functions, e.g., read-only memories for implementing multiplication, and the use of serial rather than parallel arithmetic. The potential for future gain in computing power through organization is very high for two reasons. First, since most of the logic elements in traditional systems do nothing most of the time, there is enormous room for improvement in their duty cycle. Better organization can reduce wire length or introduce latches to lessen the uncertainty in the arrival times of data and thus permit data to be transmitted at a faster rate, more nearly utilizing the full speed potential of the logic elements involved.

Second, the greatly reduced cost of logical circuitry afforded by the integrated circuit makes it economical to duplicate computation functions and deploy them geometrically close to the data elements on which they operate, thus avoiding the expensive and slow wires that are traditionally placed between memory and computing elements. Today's computers consist of a memory and a computing element separated by the barrier imposed by a memory bus; better organization should be able to eliminate this barrier.

FABRICATION IMPROVEMENTS

One area in which improvements in integrated circuit fabrication technology have been made is in feature size. Improvements in the absolute resolution of printing processes and in the resolution of fabrication processes have made it possible to reproduce smaller and smaller features reliably in the circuits. The features now being used by the industry are on the order of 5 microns in size, rapidly approaching the limits imposed by the 0.5-micron wavelength of visible light. Further improvement in feature size will depend on new fabrication processes. The current efforts aimed at using electron beams, ultraviolet radiation, and X-rays are a direct response to this need.

As mentioned above, improvements have also been made in the size of the circuit chips that can be produced with adequate yield. Defect densities in substrate materials, in masks, and in the replication processes have steadily decreased, improving the yield for a given chip size or, if yield must be held constant, permitting larger chip areas.

How the relationship between chip size and yield depends on feature size, particularly for very small features, is not known, and projections of future functional capability must be suspect until we know more about the defect mechanisms for submicron devices. We would like to believe that chip area can be held constant while feature dimensions are decreased dramatically. If pattern defects are mostly due to relatively large particles of dust or scratches, this will be possible. If, however, submicron devices are subject to a whole new set of defect mechanisms, the development of more complex circuits may be delayed.

Important improvements have been made in the precision with which a pattern can be replicated. Pattern replication precision should be treated in dimensionless terms, since a pattern remains the same when scaled to different sizes. The precision required for pattern replication is, of course, directly related to the number of circuit elements replicated; more precision means that more circuit elements can be "printed" at each replication step. Today's equipment provides precisions on the order of one part in 10^5. Considering that the coefficient of expansion of common metals and silicon is on the order of one part in 10^5 per degree, these precisions imply temperature compensation, careful control of mechanical loading, and very careful alignment. The precision of the existing microcircuit pattern replication capability exceeds anything available in the photographic or publication industries by an order of magnitude.

Because many circuits may be replicated by a single step, improvements in replication precision affect the economics of production and not the characteristics of the circuits themselves. Replication has commonly been done on a full wafer basis, and so improvements in precision have often been accompanied by an increase in wafer size or a decrease in feature size. It is important to identify replication precision improvements as being separate from other types of fabrication improvement, not only because the newly evolving short wavelength replication methods have different precisions from those to which we are accustomed, but also because today's precisions are approaching the fundamental limitations imposed by the dimensional stability of silicon. Thus further decreases in feature size may require that the total area of the pattern replicated in a single step be decreased so that the precision required in the replication step will not exceed one part in 10^5. We may well have reached the point where the complexity of patterns to be replicated (but not the complexity of the circuit chips) is approaching maximum. Replication patterns should begin to decrease in size with decreasing feature size, whereas until now they have been increasing in size in spite of decreases in feature size.

Wafer size is another area in which improvements have been made.

The size of the substrate wafer used as a production unit in integrated circuit fabrication has been steadily increasing over the past decade, making it possible to produce more circuits per unit of labor because more circuits can be placed on a single wafer. As long as pattern replication accuracy keeps pace with the requirements imposed by decreasing feature size and increasing wafer size, a single replication exposure per wafer can be used. However, further decrease in feature size or increase in wafer size will necessitate multiple replication steps per wafer, a prospect that may appreciably change the economics of using large wafers.