Appendix A

HOW BIG MUST AN INTEGRATED CIRCUIT CHIP BE?

Complex component interconnections are of two types: regular wiring patterns and irregular wiring patterns. Regular wiring patterns are those in which the wires are arrayed in rows or columns between the cells of an array of similar logical elements. Such regular patterns are used to implement memories, read-only memory cells, adders, array multipliers, bit maps, and a host of other useful logical functions.

Irregular wiring patterns are used when insufficient regularity is available in the function being implemented. Collections of logic gates to implement control functions for computing machinery, for example, are often implemented as irregular wiring patterns. At a higher level, irregular wiring patterns are found as the interconnections between subunits composed of regular wiring. Irregular patterns of wiring are difficult to design, difficult to inspect, difficult to certify as correct, and, as we shall see, wasteful of chip space.

In order to model the statistics of irregular wiring patterns, let us examine a random wiring model. We will assume that there are N points on a two-dimensional surface that are to be interconnected by a known, but random, pattern of wires. We shall try to estimate, given a center-to-center wire spacing, w, how much area will be occupied by the wires. We will assume for the moment that the wiring pattern involves at least two layers of wiring so that wires may cross each other, and that most wiring runs are arranged either vertically or horizontally in the available space. The statistics for a random wiring pattern will serve as an upper bound on the amount of space required for better organized wiring, since any effort devoted to the random pattern will surely pack it more closely together.

Experience with the layout of printed circuit boards, integrated circuit chips, and highway networks tells us that the critical congestion problem will occur at the center of the layout. We will therefore estimate the number of wires that cross the midline of the layout,

realizing that there must be enough space along the midline to accommodate these wires. Any wire that crosses the midline will be connecting a point or points on one side of the midline with a point or points on its other side. We will assume that the wiring layout has been done with at least enough common sense to permit a wire to cross the midline only once regardless of how many points on each side of the midline it interconnects.

We will be interested in how the expected number of midline crossings depends on the number of points connected together into a single "net" by each wire. Let us first consider nets involving only two points. Given N points to interconnect, there are N/2 such wires. Of these, one-half will cross the midline, since only in half of the cases will the two points to be interconnected lie on opposite sides of the midline. We can therefore expect N/4 wires to cross the midline. Now let us consider nets involving three points. There are N/3 such nets. Of these, one-eighth will involve exclusively points on one side of the midline and one-eighth will involve exclusively points on the other side, leaving three-fourths of the wires to cross the midline. Since $(3/4) \times (N/3) = N/4$, we can again expect N/4 wires to cross the midline! For nets of four points, the expected number of crossings is $(1 - (1/16) - (1/16)) \times (N/4) = 7N/32$, again very close to N/4. In fact, as Table 4 shows, the expected number of midline crossings is a very slowly varying function of the number of points in the net. For nets of most interesting sizes, we can therefore conclude that *given N points to interconnect, about N/4 wires can be expected to cross the midline of the layout.* This result was published, with embellishments, by Sutherland and Oestreicher (1973) in a paper entitled: "How Big Should a Printed Circuit Board Be?" It is a remarkably simple and powerful result.

Knowing how many wires will cross the midline of a random wiring layout enables us to determine how much space to provide for them. Naturally, any layout more systematic than random will require less space, and so we have an upper bound. Sutherland and Oestreicher successfully used their result to choose the size and component count of a family of printed circuit boards in such a way as to make the layout

Table 4

EXPECTED NUMBER OF ESSENTIAL MIDSECTION CROSSINGS
AS A FUNCTION OF NET SIZE

Net Size	Expected Crossings per Net	Expected Crossings
n	$C = 1 - P_1^n - P_2^n$	$W_m = \frac{N}{n}(1 - P_1^n - P_2^n)$
2	$1 - 1/2^2 - 1/2^2 = 1/2$	$\frac{N}{2} \times 1/2 = \frac{N}{4} = 0.25N$
3	$1 - 1/2^3 - 1/2^3 = 3/4$	$\frac{N}{3} \times 3/4 = \frac{N}{4} = 0.25N$
4	$1 - 1/2^4 - 1/2^4 = 7/8$	$\frac{N}{4} \times 7/8 = \frac{7N}{32} = 0.2185N$
5	$1 - 1/2^5 - 1/2^5 = \frac{15}{16}$	$\frac{N}{5} \times \frac{15}{16} = \frac{15N}{80} = 0.188N$
N	1	$\frac{N}{N} \times 1 = 1 = 1$

problem easy. More important, however, is that this result provides us with an understanding of the growth laws for wiring complexity.

To consider how the area occupied by wiring changes with complexity, let us determine the area per point interconnected on a two-dimensional surface that is occupied by wiring. If there are N points to interconnect, there will be N/4 wires crossing the midline of the layout, and the layout must therefore be $(wN/4)^2$ in area if the wire center-to-center spacing is w. For each point interconnected, then, an area of $(w/4)^2N$ will be required for wiring. As long as the size of the points interconnected is larger than $(w/4)^2N$, the points interconnected will occupy an area larger than the wiring. As the number of points to be interconnected is increased, the *area per point* occupied by wiring increases; through no fault of the individual interconnection points, the cost of interconnecting *each* of them increases linearly with their numbers. When enough points are involved (a remarkably small number) so that $(w/4)^2N$ exceeds the size of an individual point, the area required for the layout will be dominated by the area occupied by wiring. This is the regime in which all integrated circuits are

designed, in which many printed circuits lie, in which the back panels (Semore Cray's "mat") of the largest computers are built, and which causes most of downtown Los Angeles to be paved with overcongested freeways.

Relief from the congestion of two-dimensional wiring can be obtained by resorting to three dimensions. Obviously, providing more levels of wiring serves the same purpose as reducing wire spacing, w, if the points to be interconnected are still arrayed in a plane array. If, however, we had a mechanism for building truly three-dimensional circuits similar to the biological circuits found in the human nervous system, the growth law would be more favorable.

For a three-dimensional arrangement of N points, again N/4 wires can be expected to cross the midplane. Each such wire and the space around it, let us say, has a cross-sectional area of w^2, and so a cube whose side is $w(N/4)^{1/2}$ on a side will suffice to hold the wiring. Such a cube has volume $w^3(N/4)^{3/2}$, of which $(w/2)^3N^{1/2}$ must be assigned to each point interconnected. In three dimensions, then, the volume needed for random wiring attributable to each point interconnected increases only as the square root of the number of points interconnected; whereas in the plane, the area for random wiring attributable to each point increases linearly with the number of points interconnected.