MEMOREX 7100

SYSTEM CONTROL AND DISPLAY PANEL

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1.0   INTRODUCTION

The system control and display panel has seven basic functions:

a)   To control the mode in which the CPU operates or else halt it.

b)   To display the contents of various registers on 16 data lites.

c)   To alter the contents of any of four registers with 16 data switches.

d)   To read and write into the main memory.

e)   To control the loading of initial programs for various I/O devices.

f)   To display a parity error condition and allow the operator to reset it and restart the CPU.

g)   To allow the operator to reset the system.

These functions are described in more detail in the subsequent sections.

2.0   MODE ROTARY AND START TOGGLE SWITCHES

a)   The PROCESS position allows the processor to run uninterrupted by the panel as soon as the START switch is actuated.

b)   The MICROADDRESS HALT (MUX) position causes the processor to run as soon as the START switch is actuated. Prior to this, the DATA SWITCHES should be set to the sum of the desired halt micro address plus one. The processor will then halt one minor cycle after the MUX reaches the desired address. This leaves the Micro Instruction Register (UIR) loaded with the micro code of the desired address.

If the START switch is then actuated, the processor will

continue running and again stop one minor cycle after the MUX reaches the desired address i.e., one less than the DATA SWITCH setting. If the DATA SWITCHES are changed while the processor is halted, nothing happens until the START switch is re-actuated. The processor then runs and again stops one minor cycle after the MUX reaches the new desired address which is one less than the new DATA SWITCH setting. If a memory cycle is still in process after the last step of the above run, it will continue until completion, including the loading of the MDR in a read operation.

c)   The MEMORY ADDRESS HALT (MAR) produces the same operation as in 1 b) above except that the MAR replaces the MUX and the DATA SWITCHES are set to the exact halt address rather than one increment higher.

d)   The SINGLE MICRO CYCLE position causes the processor to halt. The START switch gates 1 minor cycle clock to the processor each time that it is actuated. If a memory cycle is started by any one of these single steps, it will continue until completion, including the loading of the MDR in a read operation.

e)   The SINGLE MACRO CYCLE position causes the processor to halt. Actuating the START switch gates as many minor cycle clocks as are required in the microcode to execute the macro insturction. When the processor halts , it leaves the Micro Instruction Register (UIR) loaded with the micro code of the next macro instruction start address. All memory cycles are completed.

3.0 HALT SW

The HALT switch stops the processor until the START or IPL switch is actuated.

4.0 ALTER REG/MEMORY WRITE TOGGLE SWITCH WITH DISPLAY/ALTER ROTARY SWITCH IN 1 OF 4 REGISTER POSITIONS

If the processor is in the halt condition and the DISPLAY/ALTER rotary switch is in any one of the four register positions -- UPNT, UIR, MAR, or MDR -- then

a) If the ALTER REG/MEMORY WRITE switch is reset, the DISPLAY/ALTER rotary switch reads the contents of the selected register on to the 16 DATA LITES. An 'on' lite indicates binary 1.

b) If the ALTER REG/MEMORY WRITE switch is actuated, the contents of the 16 DATA SWITCHES are loaded into the register selected by the DISPLAY/ATLTER rotary switch.

5.0 ALTER REG/MEMORY WRITE AND MEMORY READ TOGGLE SWITCHES WITH DISPLAY/ALTER ROTARY SWITCH IN MEMORY POSITION

If the processor is in the halt condition and the DISPLAY/ALTER rotary switch is in the MEMORY position, then the DATA LITES will display the source addressed by a GSD or SCB micro instruction in the UIR. If neither of these insturctions is present, the lights will be out. No destinations will be enabled.

a) If the ALTER REG/MEMORY WRITE switch is actuated, the MDR contents will be written into main memory at the MAR address.

b) If the MEMORY READ switch is actuated, the MDR will be loaded by the contents of the main memory at the MAR address.

6.0   IPL SWITCH

Prior to actuating the IPL switch, the operator is expected to set the DATA SWITCHES to a code corresponding to the selected I/O device. The IPL switch halts and resets the system and then sets the UPNT to a pre-determined starting address for the initial program loading routine. The processor starts running again after actuation of the START switch.

7.0   HALT LITE

The HALT lite (LED) goes on whenever the system is in the halt condition regardless of what caused it.

8.0   PARITY ERROR

A main memory read parity error causes the processor to stop and the MEMORY PARITY CHECK lite (LED) to go on. Actuation of the CHECK RESET switch turns the lite off. The processor continues immediately after the START switch is actuated. During the un-reset parity error period, the MODE, START, ALTER and MEMORY READ, and IPL switches are disabled but the DISPLAY/ALTER SW may be used for display only.

9.0   DATA LITES

Light emitter diodes (LEDs) are used for the 16 DATA LITES. When the processor is in the halt condition, they display various sources, as described in Section 4 a) and 5, above. If the processor is running, the DATA LITES dynamically display the data on the processor source and destination BUS.

10.0 SYSTEM RESET

The SYSTEM RESET switch resets the processor registers, latches and flip flops. The main memory is not reset.

DATA LITES

○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○

DATA SWITCHES

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

MEMORY
PARITY
CHECK ○

HALT ○

MODE SW
PROCESS

MEMORY
ADDRESS
HALT
(MAR)

SINGLE
MACRO
CYCLE

MICRO
ADDRESS
HALT
(MUX)

SINGLE
MICRO
CYCLE

DISPLAY/ALTER SW
MEMORY

MAR

MDR

UIR

UPNT

CHECK
RESET

SYSTEM
RESET
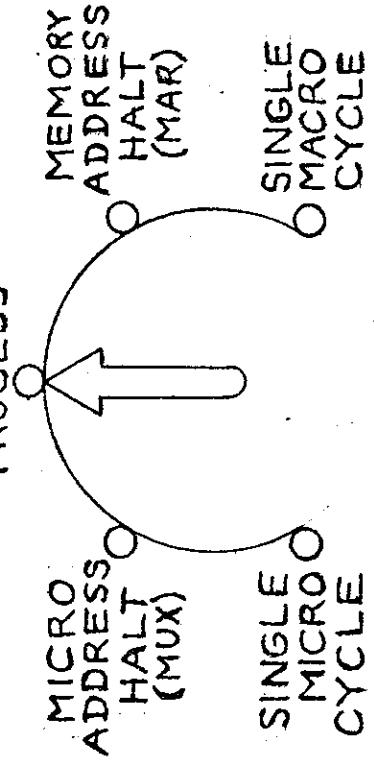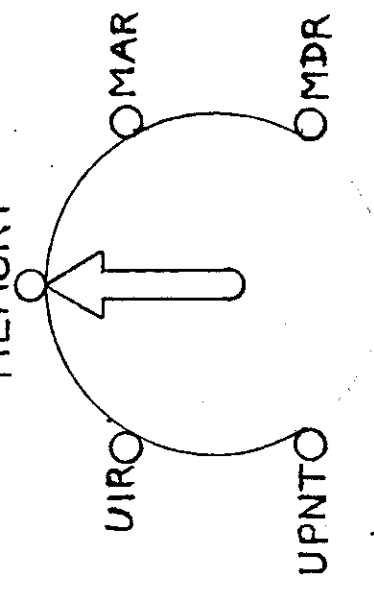
START

ALTER REG/
MEMORY WRITE

MEMORY
READ

IPL

HALT

POWER

7100 CONTROL
& DISPLAY PANEL

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