MEMOREX 7100

SYSTEM ARCHITECTURE

J.A. MILLER

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INTRODUCTION

The 7100 system consists of four separate subsystems, the CPU, Control and Display (C&D), Memory, and I/O (See Figure 1). The CPU is a microprogrammed general purpose processor using a 16 bit microinstruction word. It has a 16 bit data path for 2's complement binary arithmetic, and several special purpose and general purpose registers. The C&D subsystem is the panel lights and switches used to manually control and monitor the system. The memory subsystem consists of a maximum of 32768 16 bit words of MOS-LSI storage. The memory may be referenced on either a word or byte basis. The I/O subsystem consists of a number of device adapters logically integral with the CPU, each of which may control one or more I/O devices. These I/O adapters may access memory directly without going through the CPU. Each of these component subsystems is described in detail elsewhere.

These subsystems are interconnected via two independent data paths, the memory bus and the micro bus. In addition, an interrupt system connects the I/O subsystem with the CPU. The purpose of this section is to describe in general the interaction of the subsections via these busses and control lines, and to discuss the overall 7100 system timing.

THE MEMORY BUS

The memory bus is the path whereby the elements of the system (the CPU and the various I/O adapters) can access the memory subsystem. The interface to the memory bus is described in detail in the memory subsystem writeup.

Since several elements may desire concurrent access to memory, these elements may not access memory directly, but rather must request that

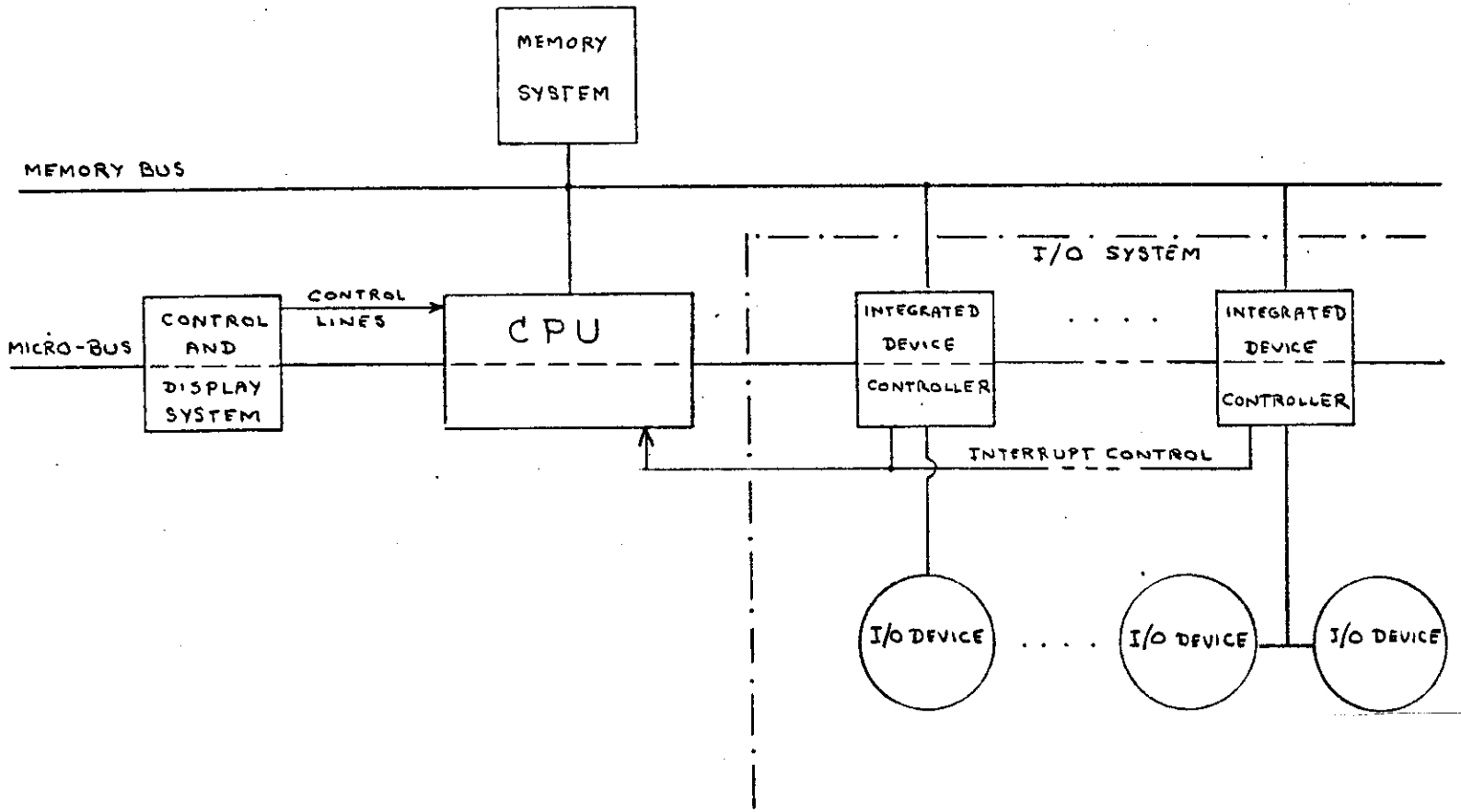

FIGURE 1. 7100 SYSTEM ARCHITECTURE

access first. The memory bus controls access to memory on a fixed priority basis. Since each element cannot control when access to memory is granted, the memory bus provides controls back to the elements that indicate both when access has been granted, and when the requested operation is complete.

THE MICRO BUS

The micro bus connects the C&D and I/O subsystems with the CPU. It provides a direct data and control path between those two subsystems and the CPU. The relationship between the CPU and C&D subsystem is rather special and is described in detail in the C&D writeup. It is sufficient to say that the C&D subsystem is permitted some degree of control over the CPU and the microbus.

The interface between the I/O subsystem and the microbus is described in the I/O writeup. To each of the device adapters, the microbus appears as an 8 bit address bus, a 16 bit data bus, and read and write control lines. There are no interlocking signal sequences nor any bus control lines returning from the device adapters to the CPU. The CPU retains complete control over the micro bus at all times. The device adapters use the system clock to control their bus operations.

Within the CPU the micro bus becomes the internal CPU microbus. Operations over the microbus to the I/O subsystem are the same as operations between the internal components in the CPU. Indeed, the CPU contains sets of registers that, for microprogram purposes, may be dedicated to the individual I/O adapters.

The general register address space within the CPU admits of 256 addresses. These may be viewed as 16 groups of 16 registers each. (16 column addresses X 16 row addresses). There are not actually 256 registers in the CPU. Those addresses that have no associated registers become operations directed to the I/O subsystem.

The 8 bit register address is formed of two components. The 4 low order bits (row address) reference one of the 16 registers within a group, and arise directly from a microinstruction. The 4 high order bits (column address) reference a register group, and arise from either the X (extended register pointer) register or the P (priority interrupt) register of the

THE INTERRUPT SYSTEM

The priority interrupt system consists of an interrupt request line for each device adapter. These lines enter the CPU where a priority encoder encodes the address of the highest priority device adapter whose request line is active. This address is loaded into the P (priority interrupt) register under microprogram control. Since P also controls the register addressing this action also permits the CPU to direct I/O operations at the interrupting device adapter. The column address recognized by a device adapter must correspond to its interrupt request line.

SYSTEM TIMING

The basic clock that is used throughout the system is a 400 nanosecond clock. This clock is available to all subsystems within the 7100.

Within the CPU this clock is used for microcycle timing. It is the time required to execute one microinstruction.

The memory subsystem works on a 1.2 microsecond cycle time. This

1.2 microsecond cycle represents 3 system clock times. The memory may start on any system clock pulse.

The system clock is also sent to the device adapters that comprise the I/O subsystem. It may there be used in any way the adapter desires. It must be used to control information passing between the CPU and the adapter via the microbus.

TABLE 1

7100 SYSTEM SPECIFICATIONS

SUMMARY

o MEMORY SIZE	Up to 64K bytes (128K bytes with option)
o MEMORY WORD SIZE	16 bits + 2 Parity bits
o MEMORY SPEED	1.2µs cycle .8µs access
o DIRECT MEMORY ACCESS	Yes, up to 7 modules
o DMA TRANSFER RATE	750K bytes/sec.
o MEMORY TYPE	MOS-LSI (2048 bit chips)
o PROCESSOR CYCLE TIME	400 ns
o PROCESSOR REGISTER FILE	16-16 bit registers
o MICRO-INSTRUCTION WORD	16 bits
o PROCESSOR TECHNOLOGY	T^2L Series 74
o I/O SYSTEM	Direct & DMA
o I/O CONTROL UNITS	7 max
o INTEGRATED ADAPTERS	Yes, up to 7
o DEVICE ADDRESSING	Through register file
o I/O TRANSFER RATE	30KB direct, 750KB DMA