MEMOREX 7100

MEMORY SYSTEM

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1.0 SYSTEM MAIN MEMORY

The system main memory (memory) is a MOS RAM data storage device. The memory system utilizes a memory bus configuration, servicing up to eight different devices on the bus. The highest priority on the bus is dedicated to the memory refresh circuitry.

The MOS RAMs that comprise the memory are 8K 9 bit byte modules that can be expanded to a total memory size of 128K bytes. One bit of each byte is for odd parity. Memory access time is 800 nanoseconds. Memory cycle time is 1.2 us. The memory cycle starts on the first system minor cycle after a memory request is raised* by any device on the memory bus.

2.0 MEMORY PRIORITY

Any one of eight different devices can request a memory cycle. However, the highest priority (0) has been dedicated to the memory refresh circuitry, the purpose of refresh is explained in 5.4. The remaining seven devices are assigned priorities as listed in Table 1.

TABLE 1

MEMORY PRIORITY ASSIGNMENTS

PRIORITY	DEVICE
0	Memory Refresh
1	To Be Determined
2	
3	
4	
5	
6	
7	

*The use of the words "raised" or "goes up" should be interperted to mean the subject signal or condition becomes true. In order to determine actual logical voltage levels reference must be made to the first level logic diagrams.

The memory priority logic determines the highest priority device with and active memory request and gates its address out on the Select Address Bus. This notifies the requesting device that a memory cycle has been granted and the memory cycle begins.

3.0 MEMORY MODE CONTROL

The two signals WR HI and WR LO are generated by the memory user and places the memory in the proper mode as shown in Table 2. In a byte write mode memory address bit 15 is decoded into WR HI and WR LO. A full memory write (FMW) or a read are also encoded into WR HI and WR LO. This encoding is done by the user. Memory address bit 15 does not go to the memory. WR HI and WR LO are treated as part of the Memory Address Bus (MAB).

TABLE 2

ENCODING OF WR HI AND WR LO

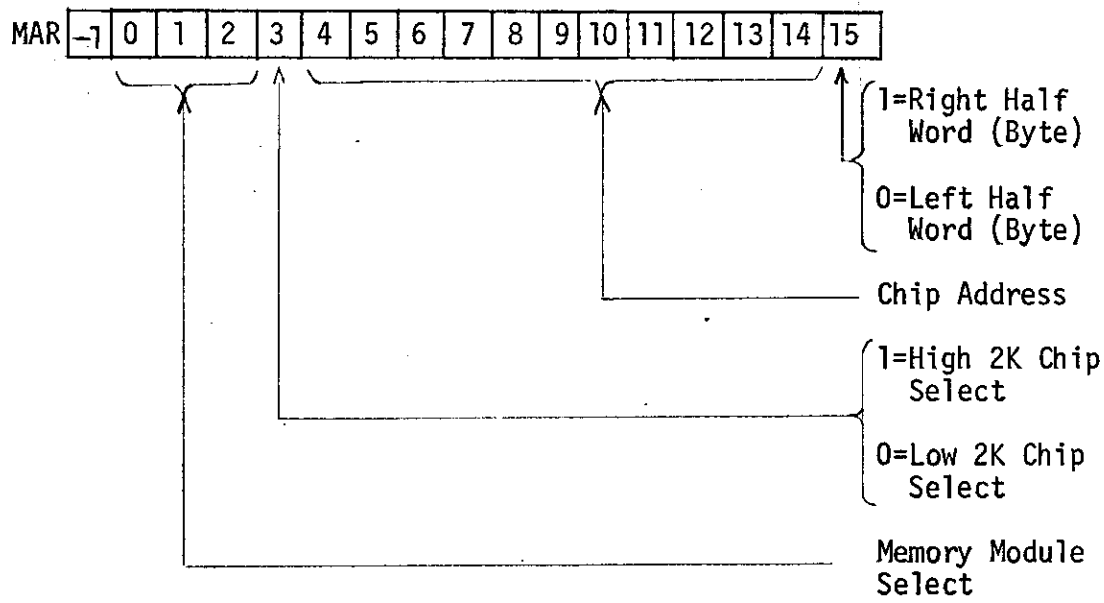
		RESULT	
	MAB 15	WR HI	WR LO
BYTE WRITE	0	0	1
	1	1	0
FMW	X	1	1
READ	X	0	0

4.0 MEMORY ADDRESSING

During normal CPU operation, the address of the desired memory location is placed in the Memory Address Register (MAR) of the device requesting a memory cycle. When a device is selected, the contents of its MAR are placed on the Memory Address Bus which goes to all the memory modules and selects the appropriate module and byte. The format of the memory address is shown in Figure 1.

FIGURE 1

MEMORY ADDRESS FORMAT

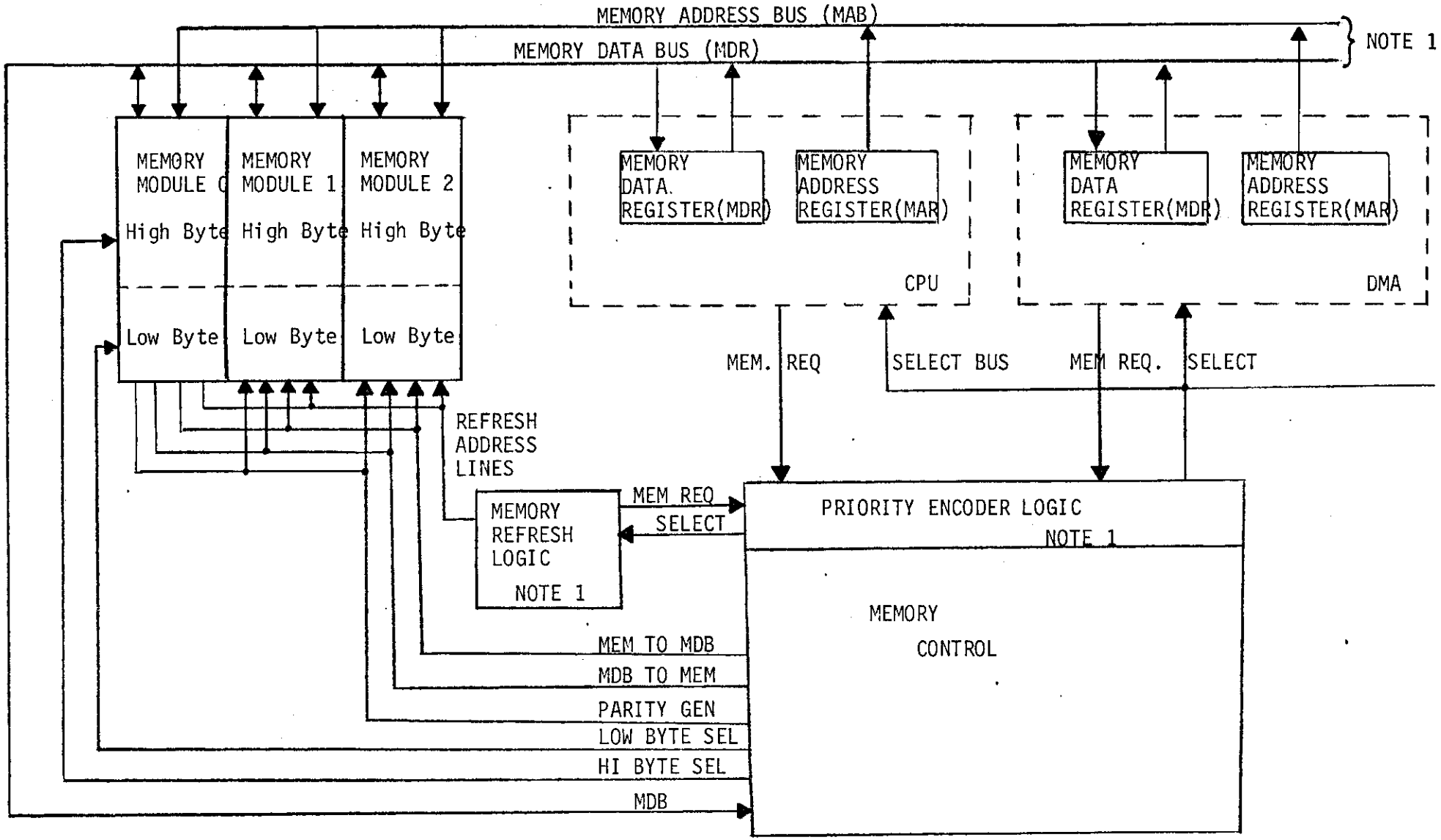


5.0 MEMORY OPERATION

The following paragraphs and Figure 2 provide a functional description of the main memory operation.

5.1 READ

The address of the memory location to be read is placed in the MAR of the device requesting a memory cycle. The requesting device also generates a memory request (MEM REQ), that is sent to the PRIORITY ENCODER LOGIC. The address of the requesting device with highest priority is placed on the Select Address Bus. The select address is decoded by the requesting device and is interpreted to mean that a cycle is granted. After a device is selected, its MAR is gated to the MAB to address the desired memory location. When the Memory is ready to transfer data, the memory control logic generates MEM DATA GATE. The generation of MEM DATA GATE cuases the contents of the



NOTES:
1. MEMORY REFRESH is permanently connected to the highest priority (0). Therefore, a maximum of 7 additional devices can be connected to the MAB and MDB.

7100 MEMORY SYSTEM, Simplified Block Diagram

FIGURE 2

addressed memory location, to be placed on the Memory Data Bus (MDB). Parity is checked by the memory control logic to ensure that the data has correct odd parity. If incorrect parity is detected, READ PARITY ERROR is generated. At the fall of MEMORY DATA GATE the data on the MDB is read into the appropriate device MDR. The memory always reads a full word.

5.2 MEMORY WRITE

After the user's MDR and MAR are loaded, the user generates a memory request (MEM REQ) that is sent to the PRIORITY ENCODER LOGIC. The address of the highest priority requester is placed on the SEL ADR BUS. When the user decodes his address, the appropriate MAR and MDR are gated to the memory buses. The memory control logic then examines the data on the MDB and generates the correct odd pairty for one or both bytes, depending on the type of write operation. After the correct parity is generated, MEMORY DATA GATE causes the data on the MDB and generated parity bit(s) to be written into the addressed memory location. When MEMORY DATA GATE returns to the inactive level, the selected device is disconnected from the memory buses and the write operation is complete.

5.3 WRITE HALF WORD

The half word write operation is similar to the full word write except MAR 15 is decoded to determine which half of the memory is to be written. The decoded MAR 15 generates either WR HI or WR LO and the appropriate byte with correct parity is written into memory.

5.4 MEMORY REFRESH

The memory stores a bit by charging or discharging a capacitance. Because these charges leak off the memory must be rewritten or

"refreshed" every 2 ms. To accomplish refresh the 32 low order addresses must be generated and a write cycle with the WRITE signal inactive is executed. This is accomplished by the memory refresh logic. Every 128th cycle, the Refresh Address Flip Flop (REF ADD FF) is set. This generates the highest priority memory request, which is sent to the PRIORITY ENCODER LOGIC.

The address of the refresh requestor will be placed on the Select Address Bus. The column address is generated by the REFRESH ADR CTR and is placed on the low order memory address lines (MAB 10 thru MAB 14). A memory cycle is executed with chip enable and write inactive. T_5 resets the REF flip flop. The trailing edge of REF increments the REF ADR CTR by one, leaving it ready for the next Refresh Cycle in 60 microseconds.

6.0 MEMORY TIMING

Figure 4-3 contains the timing of all memory operation. The memory is able to interface to the various users because it is time bound to them by the system clock shown at the top of Figure 4-3. PH1, PH2, PH3, and chip sel, are signals which are used for "housekeeping" within the memory chip itself and will not be treated in this document.

When a user desires to access the memory that user raises MEM REQ during the shaded time shown in the figure. All MEM REQ's must be stable 200ns before the next clock pulse. The priority encoder places the address of the highest priority requester on the SEL ADR bus. The 200ns is required to allow SEL ADR to settle and be decoded by the users. At the fall of the next clock pulse the highest priority requestor may begin memory access. The memory

control activates MEM BUSY. MEM BUSY is used internally to disable the priority encoder once a user has been given memory access. A selected user must have a valid address on the MAB and WR HI and WR LO stable 50 ns after selection, this allows 100 ns bus settling time. WR HI and WR LO are explained in Section 3, MEMORY MODE CONTROL.

MEM DATA GATE is used internally to gate the memory to the MDB in the case of memory read of gate the MDB into the memory in the case of memory write. Determination of memory mode (read or write) is explained in Section 5.

The signals labeled DATA IN TO CHIP and DATA OUT OF CHIP are for reference only showning the time relationship of the actual data transfer. The times at which data msut be on the MDB for a system concept are noted on the MEM DATA GATE as explained previously in this section.

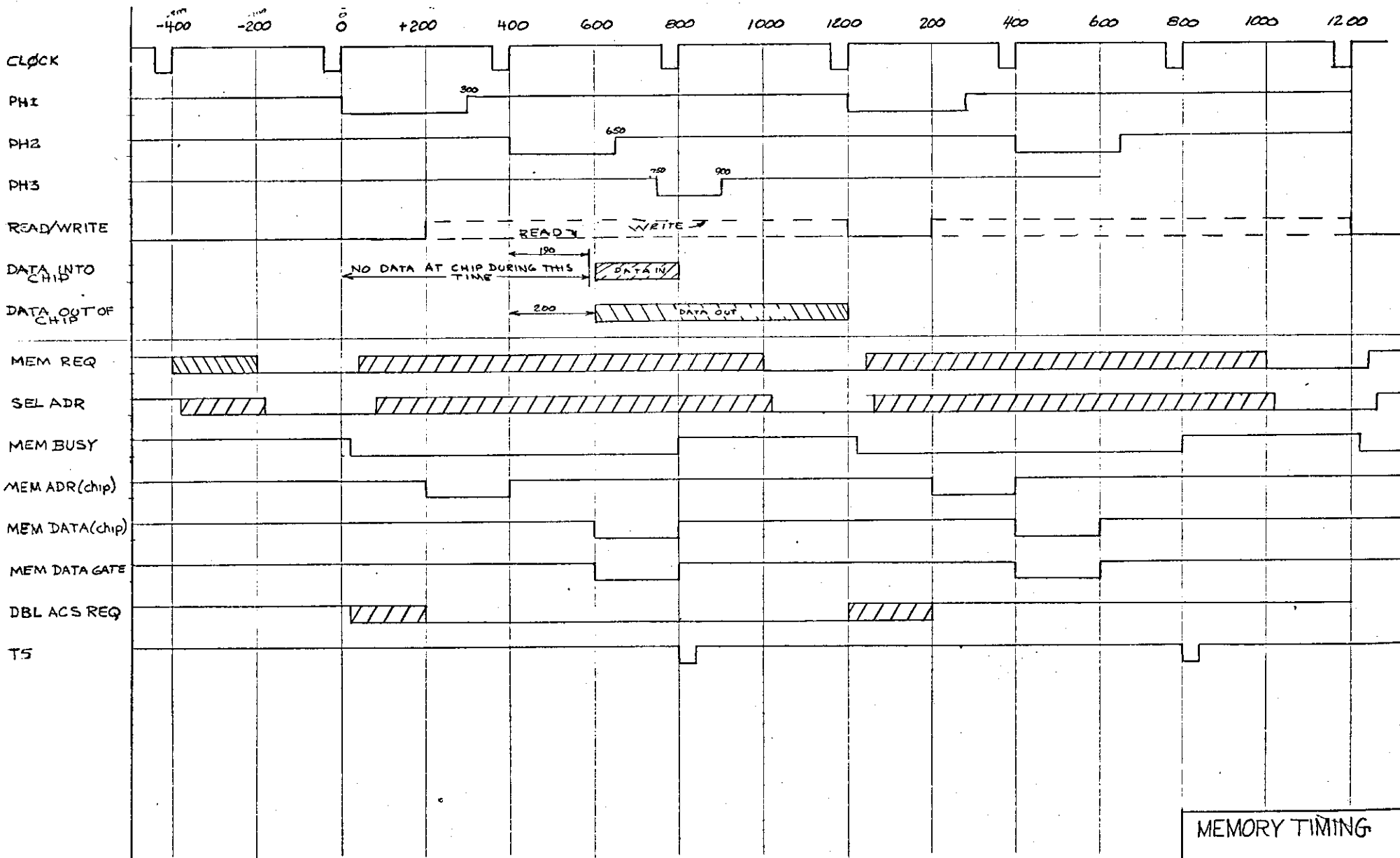
7.0 DOUBLE ACCESS

DOUBLE ACCESS provides two consecutive memory cycles either read or write. DOUBLE ACCESS is initiated when the CPU executes a TEST READ (TSR) port operation. The purpose of DOUBLE ACCESS is to enable micro-code implementation of a TES and SET function. To accomplish DOUBLE ACCESS the user raises double access request (DBL ACS REQ) after selection. DBL ACS REQ must be held up until the MEM BUSY line goes up for the second memory access cycle. The SEL ADR lines will operate normally during the first memory cycle, but no address will appear on the SEL ADR lines for the second cycle. It is not necessary for the user to raise his memory request for the second memory access. Once a double access has been granted the second cycle will usurp any requestor including refresh.

8.0 SECOND LEVEL LOGIC

The following second level logic prints are included:

MEMORY MODULE	40.10
MEMORY CONTROL	40.20



NOTES:
1. Down level is always true, unrelated to schematics
2. DIAGONAL LINES INDICATE DON'T CARE REGION

FIG.4-3 MEMORY TIMING