MEMOREX 7100

INTRODUCTION

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The Memorex 7100 System is the result of a three month design effort by the 7100 Design Team. The primary charter given the team was to "design a processor building block which could be economically used across a variety of product lines".

The primary design parameter was cost. The cost must be low enough so that the processor can be used in several market applications. However, performance of the 7100 System when used as a MRX30 is required to equal an IBM System/3. Thus the design centered around developing a minimum cost CPU which would enable the 7100 System to have the required performance.

The 7100 CPU is an inexpensive micro-programmed processor which gives the 7100 System the required performance. It has been tailored to operate in a communications oriented environment, and may be used in non-programmable applications as well as programmable ones. It contains the hardware necessary to operate under OPSYS1, thus giving the 7100 System upward compatibility with the MRX40 and MRX50 when used as a general purpose small commercial batch system.

The 7100 System design is based on implementation in T^2L logic. The use of MOS-LSI for various components of the system is under investigation.

This Memorex 7100 System Reference Manual is a collection of papers by the members of the 7100 Design Team which give a detailed description of the components of the 7100 System. Included are detailed analyses of system performance and cost.