SPECIAL REGISTERS

The set of status bits, control bits, and auxiliary registers required for the proper functioning of the MPM constitute the set of special registers. The designation of these registers is shown in Table 1.

Special registers S^{20} through S^{31} are sources of 0's; information loaded into them is not recoverable. Although all special registers are nominally 24 bits in length, not all special registers have 24 physical positions; the unused bits are noted in Table 1. If any register or bit which does not exist in the physical embodiment is addressed as a source operand, the value 0 is supplied; thus, if it is addressed as a result operand, the information is lost.

The special registers S^{3} through S^{31} are accessible only when the processor is in the supervisory mode. If these registers are addressed when in the problem mode, a privileged exception occurs, exception bit PV is set to 1, and the execution of the offending instruction is suppressed in such a way that the contents of all registers remain unchanged.

Each bit position of special registers PX, PM, SX, SM and MS has individual significance to delineate an exceptional condition, a mask, a mode, or machine status. The significance of these bits and their mnemonics are shown in Tables 2, 3, 4, and 5.

The contents of special registers IRA, EBA, and parts of MS have significance only when an interruption occurs. A complete discussion of these registers is given in the chapter "MPM Interruptions".

Special registers GP^{0}, GP^{1}, GP^{2}, and GP^{3} are not reserved for a particular function, but rather may be used as general purpose registers when the processor is in the supervisory mode. Unlike the remainder of the special registers, they are never altered or used except when explicitly addressed.

Special registers are used as operands in the instructions shown in Table 6 (instructions which may cause an exception bit to be set in PX or SX are not included).

Special Registers

Number	Name	Mnemonic	Length in bits	Unused bit positions	Privileged
0	Condition	C	24	-	no
1	Problem Exception	PX	21	21 through 23	no
2	Problem Mask	PM	21	21 through 23	no
3	Supervisory Exception	SX	11	11 through 23	yes
4	Supervisory Mask	SM	11	11 through 23	yes
5	Problem Normal Key	PNK	12	0 through 11	yes
6	Problem Alternate Key	PAK	12	0 through 11	yes
7	Supervisory Normal Key	SNK	12	0 through 11	yes
8	Supervisory Alternate Key	SAK	12	0 through 11	yes
9	Interruption Return Address	IRA	24	-	yes
10	Effective Branch Address	EBA	24	-	yes
11	Machine State	MS	16	16 through 23	yes
12	Cycle Count	CYC	24	-	yes
13	Instruction Count	INC	24	-	yes
14	Timer	TIME	24	-	yes
15	External Signal	ES	24	-	yes
16	General Purpose	GP^0	24	-	yes
17	General Purpose	GP^1	24	-	yes
18	General Purpose	GP^2	24	-	yes
19	General Purpose	GP^3	24	-	yes

TABLE 1

Problem Exception (S^1) and Mask (S^2) Registers

Number	Name	Mnemonic
0	Index Divide by Zero	XDZ
1	Add Overflow	AO
2	Add Underflow	AU
3	Multiply Overflow	MO
4	Multiply Underflow	MU
5	Divide Overflow	DO
6	Divide Underflow	DU
7	Shift Overflow	SO
8	Unnormalized Operand	UO
9	Unnormalized Divisor	UD
10	Illegitimate Operand	ILO
11	Zero Fraction	ZF
12	Low Significance	LS
13	Overflow Warning	OW
14	Underflow Warning	UW
15	Condition Check	CC
16	Address Boundary Violation	BV
17	Illegitimate Instruction Code	IIC
18	Privileged Instruction	PV
19	Register Specification	RS
20	Pause and Interrupt	PI

TABLE 2

Supervisory Exception (S^3) and Mask (S^4) Registers

Number	Name	Mnemonic
0	Input/Output	IO
1	External In	EI
2	Cycle Count Zero	CZ
3	Timer Zero	TZ
4	Instruction Count Zero	IZ
5	Missing Address, Data Load or Store	MA
6	Protected Address	PA
7	Missing Address, Instruction Execution	MI
8	Directory Interrupt	DI
9	Directory Interrupt Overrun	DIO
10	Machine Malfunction	MM

TABLE 3

Machine State Register (S^{11})

Number	Name
0	Supervisory/Problem Mode
1	Disable/Enable Mode
2	Concurrent/Sequential Mode
3	Branch State
4	Branch State
5	Branch State
6	Skip State
7	Multi-precision Carry
8	Multi-precision Carry
9	Multi-precision Carry
10	Previous Supervisory/Problem Mode for Interrupt
11	Previous Disable/Enable Mode for Interrupt
12	Previous Concurrent/Sequential Mode for Interrupt
13	Previous Supervisory/Problem Mode for SVC
14	Previous Disable/Enable Mode for SVC
15	Previous Concurrent/Sequential Mode for SVC

TABLE 4

Explanation of Branch, Skip and MPC States

Branch State $S^{11}_{3,4,5}$

000	No Outstanding Branch
001	Successful Branch Outstanding
010	IVIB Outstanding
011	SVC Outstanding
100	SVR Outstanding
101	IR Outstanding
110	Unused
111	Unused

Skip State S^{11}_{6}

0	Not Skipping
1	Skipping

Multi-precision Carry State $S^{11}_{7,8,9}$

000	No Carry	
001	+ 1	
010	--	exceptional
011	--	exceptional
100	--	exceptional
101	- 3	
110	- 2	
111	- 1	

TABLE 5

Special Registers Used as Operands

Instruction	S Registers as Source	S Registers as Result
MXS, MXSO	-	any
MSX	any	-
MSXZ	any	any
ACH, ACL, SCH, SCL	MS	MS
MCX	C	-
MAC, MXC	-	C
All Logic on Condition Bits	C	C
AXT, AXCT, AXKT	-	C
SIO, SIOA, HIO, TC, RC	-	C
All Compare	-	C
All Branch-at-Exit (except BU)	C	-
All Skip	C	-
SVC	MS	MS
SVR	MS	MS
IC	MS	EBA, IRA, MS
IR	EBA, IRA, MS	MS
SCAN	-	all

TABLE 6