INPUT/OUTPUT OPERATIONS

The input/output (I/O) operations provide for the initiation, termination, and testing of data movement between storage and input/output devices. The actual data movement is controlled by channels and device control units. The T registers contain interruption and mask bits and other control and status data for channels as shown below.

The descriptions of the instructions SIO, SIOA, HIO, TC and RC given below are incomplete and specify only the basic function of the instruction. Complete descriptions of these instructions and the use of the T registers are included in the section "Input/Output Module".

T REGISTERS

Number	Name	Length in Bits	
0	Interruption Signal, Channels 0 to 47	48	Note 1
1	Interruption Signal, Channels 48 to 95	48	
2	Mask, Channels 0 to 47	48	Note 2
3	Mask, Channels 48 to 95	48	
4	Enable Search	1	Note 3
5	Channel Number	8	Note 4
6	Interruption Status I	48	
7	Interruption Status II	48	
8	Test Channel Status I	48	
9	Test Channel Status II	48	
10	Busy, Channels 0 to 47	48	Note 5
11	Busy, Channels 48 to 95	48	

Notes:

1. For the instruction MOT, the register pair $T^{0,1}$ is considered as a 96-bit register with bits numbered 0 to 95. Neither MXT nor MZT will modify $T^{0,1}$.

2. For the instructions MZT and MOT, the register pair $T^{2,3}$ is considered as a 96-bit register with bits numbered 0 to 95.

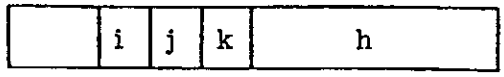
3. The unused bits of T^4 are bits 1 through 47.

4. The unused bits of T^5 are bits 0 through 39.

5. Register pair $T^{10,11}$ may be set only by channels. Hence the instructions MXT, MZT, and MOT have no effect.

Start I/O

SIO



$$\text{device number} \leftarrow X^{j}_{8,9,\ldots,15}$$

$$\text{channel number} \leftarrow X^{j}_{16,17,\ldots,23}$$

$$\text{eal} \leftarrow X^{k} + h$$

$$\text{eak} \leftarrow \text{normal key}$$

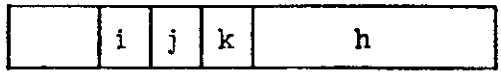
If the specified channel is not operational or is busy, bit c_i is set to 1. Otherwise, bit c_i is set to 0, and the channel command parameters (CCP) at storage location ea are sent to the channel. The CCP specifies the command to be executed by the channel and the device. The format of the CCP in storage is

command code (8), flags (4), key (12)	in location ea
address (24)	in location ea + 1
ignored (8), skip count (16)	in location ea + 2
ignored (8), transmission count (16)	in location ea + 3
FHF parameters (24)	in location ea + 4

The conditions for initiation, execution, and termination of both SIO and the command specified by the CCP are specified in the section "Input/Output Module".

Exceptions	Exception bit
in problem mode	PV
c_{24} set to 0 or c_{25} set to 1	CC

Start I/O per Alternate Key SIOA



$$\text{device number} \leftarrow X^{j}_{8,9,\ldots,15}$$

$$\text{channel number} \leftarrow X^{j}_{16,17,\ldots,23}$$

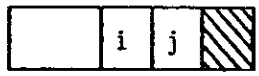
$$\text{eal} \leftarrow X^{k} + h$$

$$\text{eak} \leftarrow \text{alternate key}$$

This instruction is identical to SIO except that in forming the storage address the alternate key is used.

Exceptions	Exception bit
in problem mode	PV
c_{24} set to 0 or c_{25} set to 1	CC

Halt I/O HIO



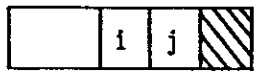
$$\text{device number} \leftarrow X^{j}_{8,9,\ldots,15}$$

$$\text{channel number} \leftarrow X^{j}_{16,17,\ldots,23}$$

If the specified channel is not operational, bit c_i is set to 1. Otherwise, bit c_i is set to 0, and the execution of the current operation at the specified channel and device is terminated. The conditions for initiation, execution, and termination of HIO are specified in the section "Input/Output Module".

Exceptions	Exception bit
in problem mode	PV
c_{24} set to 0 or c_{25} set to 1	CC

Test Channel TC

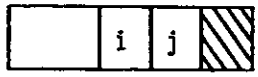


channel number $\leftarrow X^{j}_{16,17,\ldots,23}$

If the specified channel is not operational, bit c_i is set to 1. Otherwise, bit c_i is set to 0, and the contents of the channel status data (CSD) register of the specified channel replaces the contents of registers $T^{7,8}$. The operation of the channel is not effected. The conditions for initiation, execution, and termination of TC are specified in the section "Input/Output Module".

Exceptions	Exception bit
in problem mode	PV
c_{24} set to 0 or c_{25} set to 1	CC

Reset Channel RC



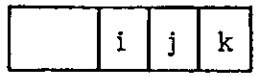
channel number $\leftarrow X^{j}_{16,17,\ldots,23}$

If the specified channel is not operational, bit c_i is set to 1. Otherwise, bit c_i is set to 0, and the specified channel and all devices attached to it are reset. The conditions for initiation, execution, and termination of RC are specified in the section "Input/Output Module".

Exceptions	Exception bit
in problem mode	PV
c_{24} set to 0 or c_{25} set to 1	CC

Move T Register to Index

MTX



$X^{i,j} \leftarrow T^{k}$

Exception

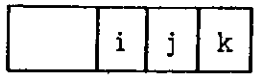
in problem mode

Exception bit

PV

Move Index to T Register

MXT



$T^{i} \leftarrow X^{j,k}$

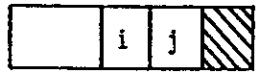
Exception

in problem mode

Exception bit

PV

Move Zero to T-Register Bit MZT



$n \leftarrow X^j$

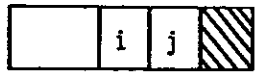
$T^i_n \leftarrow 0$

If n exceeds the length of T^i, no bit is set.

For this instruction, the register pairs $T^{0,1}$ (IO interrupt register) and $T^{2,3}$ (IO mask register) are each considered as a 96-bit register with bits numbered 0 through 95. The pair $T^{0,1}$ may be addressed by setting the i-field to either 0 or 1; similarly $T^{2,3}$ addressed by either 2 or 3.

Exception	Exception bit
in problem mode	PV

Move One to T-Register Bit MOT



$n \leftarrow X^j$

$T^i_n \leftarrow 1$

If n exceeds the length of T^i, no bit is set.

For this instruction, the register pairs $T^{0,1}$ (IO interrupt register) and $T^{2,3}$ (IO mask register) are each considered as a 96-bit register with bits numbered 0 through 95. The pair $T^{0,1}$ may be addressed by setting the i-field to either 0 or 1; similarly $T^{2,3}$ addressed by either 2 or 3.

Exception	Exception bit
in problem mode	PV