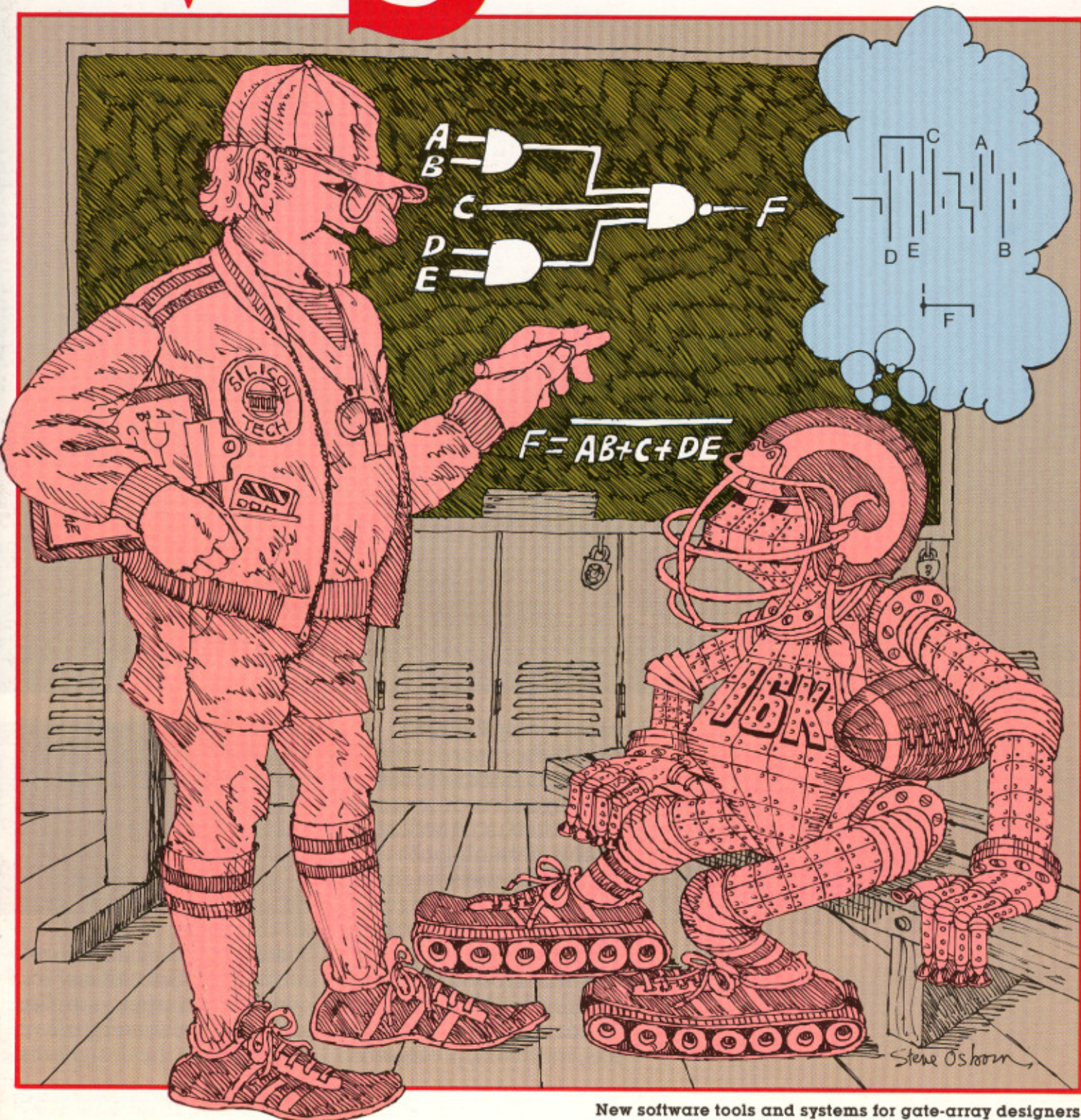


# VLSI

DESIGN

4TH QUARTER 1981



New software tools and systems for gate-array designers are changing the rules of the game.



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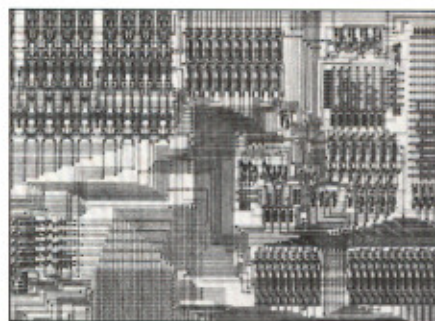
VLSI DESIGN was founded to  
explore, expand, and define the  
interrelations between very-large-  
scale integrated circuits (VLSI)  
and computer architecture,  
design strategies, costs, and  
aids, as well as the electronics  
industry as a whole. VLSI  
DESIGN is unique in that it is  
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participants in this dynamic  
field. VLSI DESIGN intends to  
be the communication focus of a  
new VLSI design community,  
encourage its development, and  
help define its directions.

# VLSI DESIGN

Volume II, No. 4, 4th Quarter 1981

## Cover

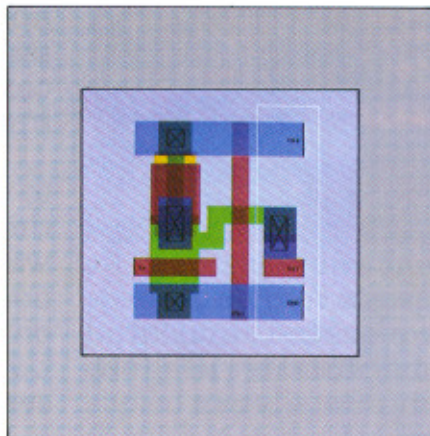
Computerized gate-array design tools are increasingly carrying the design "ball." In fact, the coming-of-age of commercially-available automated-layout tools means that the human designer will increasingly assume the coach's role.



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## Articles

### 14 A RISCy Approach to VLSI

Daniel T. Fitzpatrick, John K. Foderaro, Manolis G.H. Katevenis, Howard A. Landman, David A. Patterson, James B. Peek, Zvi Peshkess, Carlo H. Séquin, Robert W. Sherburne, Korbin S. Van Dyke  
*Computer Science Division, University of California at Berkeley*

The RISC chip is a single-chip processor designed at U.C. Berkeley. Simulation data shows the processor to be faster than both the Z8000 and the VAX.

### 22 Software for Gate-Array Design: Who is Really Aiding Whom?

Jerry Werner

This article is the first anywhere to provide a comprehensive survey of the gate-array software marketplace. Historical items are included, along with relevant technical details and current trends.

### 34 Caesar: An Interactive Editor for VLSI Layouts

John K. Ousterhout, *University California at Berkeley*

Caesar is a novel interactive layout system based on a commercially available color-graphics terminal connected to a DEC VAX. The user interface is a major advance over traditional approaches.

### 42 C-HMOS—An N-Well Bulk CMOS Technology for VLSI

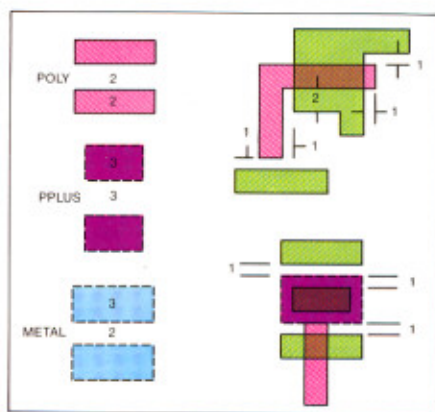
Ronald Chwang and Ken Yu, *Intel Corporation*

Intel's new CMOS n-well technology is reviewed from the point of view of the chip designer. The authors provide hints on designing with this technology.

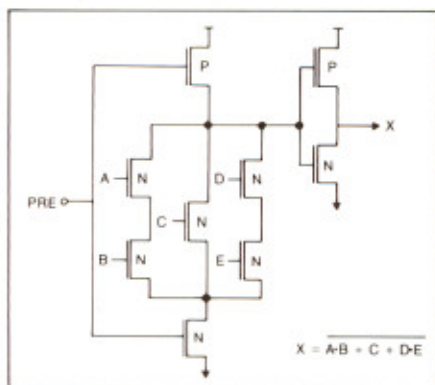
### 56 A CMOS Implementation of an Introductory VLSI Design Course

Jim Lipman, *SynMos Corporation*

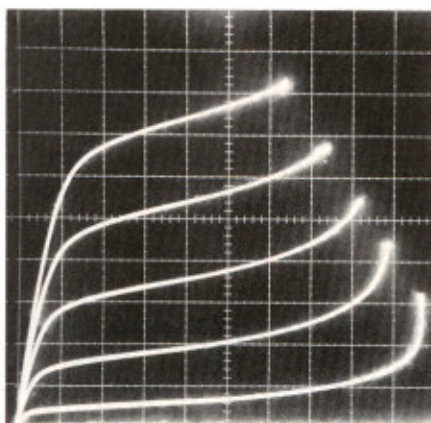
The author describes a Mead-Conway style VLSI design course based on CMOS, including lambda-based design rules for CMOS.



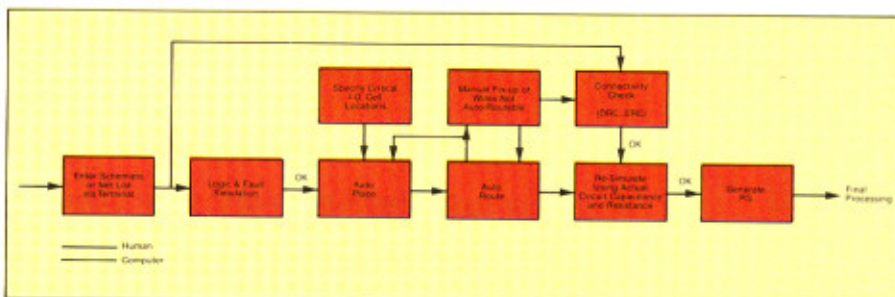
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### A New Editor . . .

I am delighted to announce that Jerry Werner has joined VLSI DESIGN as Editor-in-Chief. He will be responsible for the entire technical content of all future issues, and will have final authority on what articles and information appear in the publication. We are very fortunate to have such a highly qualified individual filling this role. Jerry is the former semiconductor editor for Electronic Engineering Times and has special skills and interests in emerging VLSI technical strategies and in techniques to improve engineering staff-to-top-management communication. Please address all correspondence concerning articles and columns to Jerry.

You can see a sample of Jerry's abilities in the article that he has contributed to this issue. "Software for Gate-Array Design: Who is Really Aiding Whom?" is a landmark article. For the first time, the history, current state, and future directions of gate-array software are recorded in one place. Among other topics, the article includes a description of the various routing techniques in use, and a listing of vendors who offer software to the marketplace. I'm sure you'll find this article worth careful reading and will want to save it for future reference. This article is just a sample of the breadth and depth of coverage we will be offering in 1982 when VLSI DESIGN starts appearing bi-monthly.

### Other Articles Focus on CMOS and VLSI Architectures . . .

Developments in CMOS technology have attracted a great deal of attention recently. But, as usual, other publications have focused primarily on fabrication. In this issue, the Technology Insight department reviews the fabrication issues, which are expanded on in two other articles that concentrate more on design-related issues.

Ronald Chwang and Ken Yu of Intel review the characteristics of the technology that affect chip designers and explain how those characteristics can best be exploited by designers. The discussion is in the context of the n-well CMOS process recently developed at Intel.

Jim Lipman of SynMos describes his experiences at Hewlett-Packard, teaching a Mead-Conway course based on CMOS technology. He includes some of the basic design structures used by chip designers, and a set of design rules based on the lambda scaling parameter.

Dave Patterson, *et al.* of U.C. Berkeley describe a very aggressive chip-design project undertaken by students and faculty. Some of the most valuable data the authors gathered concerns the performance of their processor compared to that of large systems such as the VAX, and also the amount of time spent on various steps in the design process. This information should be very useful to those trying to get quantitative information on the potential performance of VLSI chips and on the amount of work needed to design them.

As a companion piece to the above article, we have included one by John Osterhout, also of U.C. Berkeley, describing his interactive color-graphics layout system, used on the chip designed by Patterson *et al.* The novel aspects of this system include a simple and powerful user interface and the fact that it runs on a low-cost, commercially available color graphics terminal connected to a general-purpose computer (VAX 11/780). This combination provides a low-cost mode of entry into interactive layout for those already using a general-purpose computer for other applications. The user interface is so simple and natural that it lets users get started with very little training.

Because of the emphasis on design in this issue, and because of the featured position of the RISC project at U.C. Berkeley, our regular "Designer's Corner" and "University Scene" departments are absent from this issue. Both of these departments will appear regularly in 1982.



*Douglas G. Fairbairn*

Douglas G. Fairbairn  
Publisher