Survey of Silicon Foundries

Company Contact Person	Technologies Available Minimum Feature Size/Gate length (minumum metal pitch shown in parentheses) nMOS Me-G	Si-G	pMOS Me-G	Si-G	CMOS Me-G	Si-G	Bipolar	Prod. Wafer Size	Minimum Production Requirements ($ or wafers per year)	Cost Per Prototype Run (with prod. cost, if available)	Design Format from Customer
Acrian, Inc. 10060 Bubb Road Cupertino, CA 95014 (408) 996-8522 Jim Huiskens VP of Mfg.	√ 6μm (10μm)				√ 6μm (10μm)		√	3″	$10,000/yr.	nMOS: $3,000 per 25 wafers CMOS: $4,000 per 25 wafers Bipolar: $25 per wafer, per mask layer	Masks, Calma tape, PG tape
American Microsystems, Inc. 3800 Homestead Road Santa Clara, CA 95051 (408) 246-0330 Jerry Crosby Product Manager, COT Products		√ 3.5μm (nMOS I) 3μm (nMOS II) 5μm, 6μm	√ 7.5μm		√ 7.5μm	√ 5μm (CMOS I), 3μm (CMOS II) single or double metal		4″	Working plate plate input: $75,000/yr. PG or Calma input: 10 times engi- neering cost for first year	Development cost: $14,000 to $30,000	Calma tape, PG tape, working plates
ASEA HAFO 66 Bovet Road San Mateo, CA 94402 (415) 574-5400 Anders Dejenfelt Sales Manager					√ 3μm (8μm)	√ 2μm (10μm) CMOS/ SOS		3″	One batch (40 me-gate CMOS wafers or 20 CMOS/ SOS wafers)	$20,000 (incl. mask and wafer- fab charges)	Masks, PG tape, CIF (PG tape or CIF preferred)
Cherry Semiconductor Corp. 2000 S. County Trail E. Greenwich, RI 02818 (401) 885-3600 David Pryce Marketing Manager							√ linear, I^2L, optoelect.	3″	100 wafers/ month	$3000 per engineering run (10 wafers) Prod. cost: $120 to $160 per wafer (1,000 to 5,000 wafers/mo.)	Applicon tape, Calma tape, masks, scaled drawings
Citel 3060 Raymond Street Santa Clara, CA 95050 (408) 727-6562 Gary Hess Marketing Director	√ 5μm (10μm)	√ 3μm (8μm) 4μm (8μm) 5μm (10μm)	√ 5μm (10μm)	√ 5μm (10μm)	√ 5μm (10μm)	√ 3μm (8μm) 4μm (8μm) 5μm (10μm) 5μm 2-layer poly	√ Linear 6μm, I^2L 5μm	3″ and 4″	Lot: 25 wafer starts	Variable	Calma tape, masks, PG tape
Comdial Semiconductor Serv. 1230 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-1800 Gary Kennedy VP and General Manager		√ 3μm (8μm), 4μm (8μm)				√ 4μm (8μm), 4μm (8μm), 2-layer poly, 5μm (8μm)		4″	25 wafers (Comdial specializes in quick- turnaround prototyping)	$7000 to $8000 for 3μm HMOS (10 or 15 days) $7000 to $9000 for 4μm CMOS (10 or 15 days) Consult factory for other requirements	Calma tape, CIF, masks, e-beam tape
Exar Integrated Systems, Inc. 750 Palomar Avenue Sunnyvale, CA 94088 (408) 732-7970 Thruston Awalt		√ 5μm			√ 5μm	√ 5μm	√ Linear, I^2L	3″	250 wafers/yr.	Consult factory	Calma tape, masks (preferred)

Post Wafer-Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std. process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
(none)	Masks to wafers: 6 wks. PG tape to wafers: 10 wks.	Test monitors supplied by Acrian or by customer	Initial engineering review; updates as required	All	Yes	Process simulation support via PRODEM (similar to SUPREM)	(none)	Yes	Rad.-hard megate CMOS: June 1983 Si-gate CMOS (5μm): Nov. 1983
Probing, packaging, packaged-part testing	PG tape to cut-and-go's: 4 to 5 wks. Database tape to cut-and-go's: 5 to 6 wks. PG tape to packaged parts: 7 to 10 wks.	AMI process control monitor on all wafers; will add customer PCM if requested	Formal review after each phase of AMI development cycle (optional)	Available for all processes	Yes	ASPEC	In negotiation with several companies	Yes (V_T and implants)	nMOS III (2μm): 3Q83 CMOS I (shrink to 4μm): 3Q83 CMOS II (10V): 2Q83 CMOS III (2μm): 1Q84 EEPROM process: 4Q84
Probing, packaging, packaged-part testing, burn-in	PG tape to wafers: 6 wks. (CMOS) 7 wks. (CMOS/SOS) Add 3 wks. for packaging/testing	ASEA HAFO-supplied process-param. modules (PPM's) and yield-measurement modules (YMM's)	Initial review	All processes provided	Yes	SPICE 2G4 and SPICE 2G5	Process is RCA-compatible	Yes, (large order)	4-inch process line with dry processing and positive photo-resist: 4Q83
Probing, packaging, testing	8 wks. (typical): Design rule check, 1 wk.; Mask generation, 2 wks.; Fabrication, 5 wks.	Cherry-supplied PCM	Design reviews to establish circuit/process requirements	All	Maybe	ISPICE (NCSS)	Yes (not specified)	Yes	(none contemplated)
Probing, packaging, packaged-part testing	Masks to packaged parts (production parts, typical) nMOS/pMOS: 6-8 wks. CMOS: 7-9 wks.	Citel- or customer-supplied test circuit	Initial review	All	Yes	Electrical (not simulator) parameters supplied	(not specified)	Depends on individual case	4" bipolar capability: Dec. 31, 1983
Probing, packaging, packaged-part testing	Masks to wafers (prototype): 5 wkg. days (HMOS) 10 wkg. days (CMOS) Masks to tested wafers (Qty.: 500): 15 wkg. days	Comdial- or customer-supplied test device	Initial review	All	No	SPICE	Unofficially, process is compatible with several large semi-conductor suppliers	Open for discussion	3-μm p-well CMOS (6μm metal pitch): 4Q83 3-μm n-well CMOS process: 4Q83
Probing, packaging, packaged-part testing	Masks to wafers out: 4 to 6 wks. Add 2 to 4 wks. for tested devices	Exar- or customer-supplied PCM (in-house PCM preferred)	Initial review plus any required process matrices	All	Yes	(not available)	Rohm (parent company in Japan)	Yes (negotiable)	(not specified)

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Four-Phase Systems, Inc. 10700 N. De Anza Blvd. Cupertino, CA 95014 (408) 255-0900 Larry Ragle Marketing Manager	✓ 7μm	✓ 5μm	✓ 8μm		✓ 7μm	✓ 4μm		3″	(not defined)	Typical engineering qualification run: $5,000	Working plates, PG or data-base tape
General Instrument Microelectronics Division 600 W. John St., C.S. 620 Hicksville, NY 11802 (516) 733-3611 J.E. Edwards		✓ 4μm (9μm)				✓ 5μm (10μm)		4″	50 wafers	Prototype run (including mask costs): $8000 (50 tested prototypes or 5 wafers out)	Calma GDSII tape (preferred); PG tape, masks
GTE Microcircuits 2000 W. 14th Street Tempe, AZ 85281 (602) 968-4431 Fred M. McWilliams Sales Manager, Silicon Foundry		✓ 5μm				✓ 4μm, ISO^2 CMOS, 4μm	✓ Linear	4″	100 wafers/yr. (engineering qual. runs: 25 wafers)	Consult factory	Calma tape, masks, PG tape
Harris Semiconductor P.O. Box 883 Melbourne, FL 32901 (305) 729-5681 Dennis Gaetano Mgr., Mktg. Planning	✓ 5μm (15μm)		✓ 5μm (15μm)	✓ 4μm (10μm)		✓ 3μm (8μm)	✓ STL, 2-layer metal, 14μm metal pitch	4″ MOS; 3″ bi-polar	$100,000/yr.	Consult factory	PG tape or Calma tape (preferred); masks
Hughes Aircraft Co. Solid State Products Div. 500 Superior Avenue Newport Beach, CA 92663 (714) 759-2964 P. Jennifer Huffer Div. Advert. Manager					✓ 4μm	✓ 3μm		3″ and 4″	25-wafer lots	Consult factory	Calma tape, PG tape
Intel Corp. 5000 W. Williams Field Road Chandler, AZ 85224 (602) 961-8051 Bob Koehler Marketing Manager		✓ HMOSI 3.5μm*, HMOSII 2μm*				✓ 2μm* CHMOS		4″ and 6″	10,000 units/yr. (“classical foundry”)	Consult factory	Applicon tape, Calma tape
International Microelectronic Products 2830 N. First Street San Jose, CA 95134 (408) 262-9100 Bob Gardner Marketing Manager		✓ 3μm (8μm), 4μm, 5μm				✓ 3μm (8μm), 4μm, 5μm		4″	$50,000/yr.	Prod. cost (3μm CMOS): $6500 to $8500 plus mask costs	Calma tape or Applicon tape (preferred); masks
Micrel 1235 Midas Way Sunnyvale, CA 94086 (408) 245-2500 Stan Ericsson Director, Sales/Mktg.		✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ 4μm (10μm)	✓ Linear TTL	3″	25 wafer starts	Engineering run (25 wafer starts): $2500	Database tape, masks, PG tape
Micro-Circuit Engineering, Inc. 1111 Fairfield Drive W. Palm Beach, FL 33407 (305) 845-2837 Dirk Schwebe Marketing Manager					✓ 5μm (10μm)	✓ 5μm (10μm)	✓ biFET and biMOS processes; 20V, 40V, 80V	4″	Order commitment: $100,000	(consult factory)	Calma tape, CIF, masks, PG tape

*Intel uses “effective channel length” which may be a lower number than the equivalent “drain channel length” specified by other vendors.

Post Wafer-Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std. process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing burn-in	Masks to wafers: 4 wks. (typical) Add 1 wk. for assembly/test of small lots	Four-Phase or customer-supplied PCM. Will also work on a good die-per-wafer basis	"Constant" interaction	All	No	Available (not specified) but "rarely requested"	(no formal agreements)	Yes	Some 4"wafer production by 4Q83. Plans to increase volume in 4μm Si-gate CMOS process by 3Q83
Probing, packaging, packaged-part testing	Calma tape to wafers: 8-10 weeks (typical) Add 2-3 weeks for packaged devices	Electrical parameters measured on GI test structures	Initial review, follow-up reviews as required	All (3μm process specs not final as of 4/25/83)	Yes	(not available)	(no formal agreements)	Yes (within limits)	3μm Si-gate nMOS process avail. 4Q83 3μm Si-gate CMOS process avail. 4Q83
Probing, packaging	Masks to wafers: 5-6 weeks (typical)	GTE-supplied PCM	Periodic process and design reviews	All	Yes	SPICE, TEGAS	Mitel	Maybe (depends on size of order)	3μm, 2-layer metal Si-gate CMOS avail. 3Q83
Probing, packaging, packaged-part testing, burn-in	Calma tape to probed wafers: 10-12 weeks (typical) Add 6-12 weeks for packaged, tested parts	(negotiable)	Depends on customer requirements	All	Yes	SLICE (Harris' version of SPICE)	(none)	Yes (if it makes "business sense")	2μm, 2-layer metal CMOS, under development for gate arrays, should be avail. as foundry process by end of 1983
Probing packaging, packaged-part testing	PG tape to masks: 10 days Masks to finished wafers: 25 days	Standard Huges PCM	Periodic process and design reviews	All	Yes	SPICE (worst-case process modules)	Yes (not specified)	Yes (if volume warrants it)	(not specified)
Probing, packaging, packaged-part testing, characterization (skew runs)	Database tape to tested wafers (prototype run): 9-12 weeks	Intel PCM always stepped into wafer	Intel prefers to work with customers who design chips chips using the iCEL® standard cell program	All	Yes	ASPEC (usually reqs. non-disclosure agreement)	No	No	(not specified)
Probing, packaging, packaged-part testing, burn-in	Database tape to packaged/tested parts: 6 weeks (5μm) 7 weeks (3μm CMOS) (3 weeks cycle avail. at added cost)	IMP PCM (preferred) or customer-supplied PCM	Initial review plus any necessary follow-up	All	Yes	Available (not specified)	Comdial (others in negotiation)	Yes (usually for eng. prototype run only)	2-layer poly and 15V CMOS processes by 4Q83. 2-layer metal by 4Q83
Probing, packaging, packaged-part testing, burn-in	PG tape to wafers: 5-7 weeks (typical) Add 3-4 weeks for packaged, tested devices	Micrel- or customer-supplied PCM	Initial review, follow-up reviews as required	All (design rules generally supplied by customer)	No (Micrel will sign non-discl. for cust. supplied rules)	(not available)	Will modify process to be mask compatible with prime source	Yes (see left)	4" wafers by 4Q83. Schottky TTL (3-μ epi) by 4Q83
Probing, packaging, packaged-part testing	Calma tape to packaged/tested samples: 7-11 weeks	MCE-supplied PCM	Periodic process/design reviews	All	Yes	SPICE, ASPEC-G2	Yes Linear Technology Corp.	Yes	3μm oxide-isolated Si-gate CMOS by 12/83 20V dielectric-isol. bipolar by 12/83. 40V dielectric-isol. bipolar by 12/83

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Mitel Semiconductor 360 Legget Drive P.O. Box 13320 Kanata, Ontario K2K 1X5 Canada (613) 592-5630 Gene Cohen Custom Prod. Line Mgr.					√	√ 3μm, 4μm, 5μm		4″	Wafer run: 20 wafers Order: $10,000	(see left)	Calma tape, PG tape, masks
Mosfet-Micro Labs, Inc. Penn Centre Plaza Quakertown, PA 18951 (215) 536-2104 Robert O. Campbell Marketing Manager	√ 3μm	√ 3μm (also tungsten gate)	√ 3μm	√ 3μm	√ 3μm	√ 3μm (also tungsten gate)		3″	Prod. cost: $2000 (me-gate pMOS, nMOS) to $3500 (Si-gate CMOS)	(see left)	PG tape, masks
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 737-6055 Richard T. Barck Dir. MOS/LSI Mktg.	√ 5μm	√ 3μm, 4μm to 5μm	√ 8μm		√ 7μm	√ 3μm Single and dual poly, 3μm dual metal	√ I^2L, 5V Schottky; 5-100V non-Schottky; 5V gold-doped	4″ and 5″	Business per *family:* $150,000 to $200,000/yr. (Not interested in prototype business only)	Prototype lot charge (not incl. mask/test charges): $225/wafer (me-gate) $350/wafer (Si-gate)	Calma tape (preferred); Applicon tape, masks, PG tape
NCR Corporation Microelectronics Div. 2001 Danfield Court Ft. Collins, CO 80525 (303) 226-9580 Dave Newman Prod. Strategy Mgr.		√ 3μm Single or dual metal				√ 3μm (7.5μm) single or dual metal		4″	500 wafers for non-std. processing; 100 wafers otherwise	(consult factory)	Calma tape (preferred); PG tape, masks
Nitron 10420 Bubb Road Cupertino, CA 95014 (408) 255-7550 Robert Miller VP, Mktg. and Sales					√ 5μm (12μm)	√ 4μm (12μm)		3″ and 4″	$100,000/yr. (including non-recurring costs)	(consult factory)	Calma tape, PG tape, masks, reticles
Plessey 1641 Kaiser Avenue Irvine, CA 92714 (714) 540-9937 Peter Minett Product Mktg. Mgr.		√ 5μm (10μm), 6μm (12μm)				√ 2.5μm (8μm), 4μm (9.6μm), 5μm (12μm)	√ 3μm ECL, 4μm ECL	3″ and 4″	$50,000/yr.	(consult factory)	Calma tape, masks, PG tape
Polycore Electronics, Inc. 1107 Tourmaline Drive Newbury Park, CA 91320 (805) 498-8832 S.K. Leong Vice President					√ 7μm (>20V process avail.)		√ Linear, I^2L dielectric isolation combination CMOS/ linear	3″	24 wafer engineering lot	Engineering runs: $3000 to $6000 Production costs (avg.): $100/wafer (CMOS) $130/wafer (linear)	Working plates
RCA Solid State Div. Rt. 202 Somerville, NJ 08876 (201) 685-6000 Jurgen W. Scherer Mktg. Mgr., Custom Products					√ 7μm	√ 3μm, 5μm CMOS/ SOS: 3μm, 4μm, 5μm,		4″ (3″ for CMOS/ SOS)	(consult factory) (RCA offers foundry services on selected basis only)	Evaluation-lot costs: $20,000-$30,000 Tooling costs: $10,000-$20,000	Calma tape
Semi Processes, Inc. 1971 N. Capital Ave. San Jose, CA 95132 (408) 945-1500 C.B. Detrick Wafer Service Mgr.					√ 4.5μm	√ 4.5μm		3″	(not specified)	Typical cost for evaluation run (CMOS me-gate): $2500	Masks

Post Wafer-Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std. process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing	Masks to wafers: 6 weeks (typical) Add 4 weeks from PG tape; add 2 weeks to packaged parts	Mitel PCM	Technical review meetings possible	All	Yes	SPICE	GTE Microciruits	Yes (negotiable)	(not specified)
(services available locally elsewhere)	Masks to test circuits: 3 to 4 weeks	(flexible)	Interaction with MML's engineers/ technicians as required	Sells layout rules for $250	—	(not available)	(sometimes)	Yes	High-voltage MOS; also working with V-groove MOS
Probing, packaging, packaged-part testing, reliability processing	Database tape to PCM-tested wafers: 6 to 10 weeks (depending on process) For packaged parts, add 4 to 6 weeks	Standard National PCM	Initial and follow-up process/design reviews as required	All	Yes	SNAP (NSC internal)	Yes (not specified)	Yes (minor)	2μm double-metal n-well CMOS: mid 84
Probing, packaging, packaged-part testing, burn-in	Calma tape to tested wafers: 6 weeks (typical)	Prefers to step-in NCR PCM	Initial review Followup reviews as necessary	Negotiable		SPICE	Not yet (in negotiation with 3 large companies)	Yes (depends on volume)	Will be able to manufacture devices (with poly-to-substrate capacitors) for analog functions in CMOS circuits by end of 1983
Probing, packaging, packaged-part testing, burn-in	Masks to tested wafers: 4 to 6 weeks From PG tape add 2 weeks; to packaged/tested parts: add 4 weeks	Nitron PCM (preferred) or customer-supplied PCM	Initial and follow-up process/design reviews	For older processes	Yes	(not available)	Universal Semiconductor (Si-gate)	Yes (within limits)	3μm Si-gate CMOS available by 1Q84
Probing, packaging, packaged-part testing	Masks to wafers: 2 wks. PG tape to tested devices: 6 wks.	Plessey PCM	Initial review	All	Yes	SPICE	Yes (not specified)	No	2.5-μm CMOS by end of 1983
Probing, (packaging in far East and testing can be arranged)	Fast-turnaround engineering runs, masks to wafers: 2 wks. (CMOS) 3 wks. (linear) Add 2 to 3 days for sample packaging	Polycore-supplied PCM	Initial review	All	No	(not available)	(no formal agreements)	Yes	(not disclosed)
Probing, packaging, packaged-part testing, burn-in	(not specified)	RCA's Wafer Acceptance Test (WAT) criterion	Initial formal design reviews (required)	All	Yes	R-CAP	(no formal agreements)	No	(none)
Basic testing	Masks to wafers: 4 wks. (me-gate CMOS) 6 to 8 wks. (Si-gate CMOS)	Mutually agreed-upon PCM	Periodic interaction	All	For Si-gate CMOS process only		(not specified)	Yes	5″ wafer production by end of 1983

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Silicon Systems, Inc. 14351 Myford Road Tustin, CA 92680 (714) 731-7110 Bob Schultz Director, Customer Servs.					√ 7μm (12μm)	√ 3μm (8μm)	√ Junction-isolated (12V V_{CED}), 14μm	4″	$20,000/yr.	(consult factory)	Calma tape, CIF, masks, PG tape
Solid State Scientific, Inc. 3900 Welsh Road Willow Grove, PA 19090 (215) 657-8400 John J. Wunner Director of Mktg.		√ 7μm			√ 6μm	√ 3μm		4″	$250,000 over first year	$15,000 to $30,000 to produce packaged prototypes from PG tape	Applicon tape, PG tape
STC Microtechnology 2270 S. 88th St., MD G1 Louisville, CO 80027 (303) 673-4307 Lori Hiatt		√ 3μm (1- or 2- layer metal)		√ 3μm (1- or 2- layer metal)		√ 3μm (1- or 2- layer metal)		4″	500 wafers or $250,000/yr.	$10,000 for first 20 wafers	Calma tape, Applicon tape, CIF, PG tape, masks
Supertex, Inc. 1225 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-0100 Richard Siegel Vice President/Sales					√ 5μm (10μm)	√ 5μm (10μm)		4″	Lot: 24 wafers	Engineering lots: $4800 to $8400	Masks
Synertek (a subsidiary of Honeywell) 3001 Stender Way Santa Clara, CA 95054 (408) 748-7045 Dan Carlson COT Marketing		√ 2μm (6.5μm), 3μm (9μm), 5μm (10 and 11.5μm) single & double poly				√ 2μm double poly (6.5μm), 3μm (9μm) single & double poly		4″	5 wafer runs per year (20 wafers out per run)	Production cost: $250 to $400 per wafer	Calma GDSII (preferred); PG tape, masks
United Microelectronics Corp. 3056A Scott Boulevard Santa Clara, CA 95050 (408) 727-9239 Troy Speers Marketing Manager		√ 3μm (7μm)			√ 5μm (10μm)	√ 3μm (8μm)		4″	Production run: 24 wafers (engineering prototype run: 10 wafers)	Engineering wafers: $200 each (minimum 10)	Calma tape, PG tape, masks
Universal Semiconductor, Inc. 1925 Zanker Road San Jose, CA 95112 (408) 279-2830 Barry Boulton Sales Manager		√ 5μm (10μm				√ single and double poly 3μm (10μm), 5μm (10μm)		4″	500 wafers (engineering run: 50 wafer starts)	Engineering run: $15,000 plus tooling ($25,000 plus tooling without product commitment)	Calma tape, Applicon tape, PG tape, masks
VLSI Technology, Inc. 1101 McKay Drive San Jose, CA 95131 (408) 942-1810 Tony Valentino Marketing Manager,		√ 3μm (7.0μm) HMOSI, 5μm				√ 3μm n-well process via Japan source		4″	Production lots: 10 wafers Prototype runs: 5 wafers Multi-product wafers (MPW): 20 packaged, untested devices	MPW run: $5000-$7500 Typical wafer charges: (4 wks. through- put): $400/wafer (5μm nMOS) to $700/wafer (4μm CMOS)	CIF, PG tape, Calma tape, (also masks for standard processing)
ZyMOS Corp. P.O. Box 62379 Sunnyvale, CA 94088 (408) 730-8800 Cliff Vaughn COT Mktg. Manager					√ 5μm (10μm)	√ 5μm (9μm), 3μm (8μm) in devel.		4″	6-wafer prototype run plus 50 wafers/yr. (eng. proto- type run: 10 wafers)	6-wafer proto- type run: $4800 to $5300 Production volume costs: $220 to $260 per wafer	Database tape, PG tape, masks

Post Wafer-Processing Services (wafer probing, packaging, testing, etc.)	Normal Turnaround Time	Wafer Acceptable Criteria (std. process control monitor)	Technical Interaction Between Foundry and Customer	Availability of Design Rules for Various Processes	Must Customer Sign Non-disclosure Agreements	Simulator Parameters Available	Second-Source Agreements	Will Foundry Modify Process?	Processes Available Within Next 6 Months
Probing, packaging, packaged-part testing, high-reliability back-end screening	Masks to tested wafers: 6 to 8 wks.	SSI- or customer-supplied PCM	Initial design review	All	No	SPICE	(no formal agreements)	Yes (depends on volume)	Washed emitter bipolar process available 4Q83
Probing, packaging, packaged-part testing, qualification/ screening	PG tape to tested wafers: 10 to 12 wks.	Stepped-in test sites (source not specified)	Initial process/ design reviews, further assistance as required	All	Yes	MSINC (SPICE available soon)	nMOS process compatible with Standard Microsystems	Yes (depends on circum-stances)	(none)
Probing, packaging, packaged-part testing, charac-terization	Masks to tested wafers: 2 wks. From PG tape: add 1 wk. From CIF or CAD database tape: add 2 wks. To tested/pkg. parts: add 2 wks.	STC PCM	Various process/ layout/design reviews available	All	Yes	SPICE MOS2 model parameters	(available but not specified)	Yes	2μm Si-gate CMOS and nMOS processes, 1- or 2-layer metal by 4Q83
Custom handling	Masks to tested wafers: 4 to 6 wks. (me-gate) 5 to 8 wks. (Si-gate)	Supertex-supplied PCM	Process parameter reviews	All	Yes	(not available)	No formal agreements (claims to be mask compat-ible with Mitel, GTE, and AMI)	Yes	4μm Si-gate CMOS by 4Q83
Probing, packaging, packaged-part testing, burn-in	Calma tape to wafers: 10 wks. From PG tape: 8 wks. From masks: 3 to 5 wks.	Synertek PCM required on at least 3 of 5 test sites	Depends on customer requirements	All	Required for 2μm and 3μm processes	Provide SPICE simulation (but not actual SPICE model)	Some (not specified)	Yes (implant levels only)	5″wafer processing capability by 1Q84
Probing, packaging, packaged-part testing	Masks to wafers: 3 wks. From PG tape: add 1.5 wks. To packaged parts: add 1.5 wks.	PCM (source not specified)	Initial design rule exchange/ review	All	Yes	Some SPICE and ASPEC parameters available; not complete for 3μm process	Mask compatible with AMI Si-gate CMOS	Yes	3μm 2-layer metal and 3μm 2-layer poly CMOS process available by 4Q83
Probing, packaging, packaged-part testing	Masks to probed wafers: 5 wks. From PG tape: add 2 wks.; to packaged samples: add 1 wk.	Prefers Universal PCM stepped in; but will accept customer PCM	Initial review, circuit design and CAD support	All	Yes	SPICE2G	Siliconix and Nitron (others in negotiation)	No	2μm oxide-isolated CMOS by Dec. 1983
Probing, packaging, packaged-part testing	Database merge to packaged parts (MPW): 4 wks. Masks to wafers (stand-alone product): 2.5 wks.	VTI-supplied PCM	Process com-patibility and prototype verification reviews	All	Yes	SPICE, ASPEC	Ricoh Corp. (Japan)	Yes (V_T only for low volume)	2.5μm HMOSII available by 3Q83 3μm n-well CMOS in August 1983 3μm twin tub CMOS: 4Q83 2-layer metal CMOS available by end of 1983
Probing, packaging, packaged-part testing, high-temp. and mil. std. testing	Masks to wafers: 3 to 4 wks. PG tape to wafers: 5 to 6 wks. Add 1 wk. for tested prototypes	ZyMOS-supplied PCM (not proprietary; available to other IC makers)	Initial and follow-on reviews as required	All	No	Most SPICE parameters available	Intel (3-μ HCMOS) Calls older processes "industry standard"	Slight adjustments only	3-μHCMOS available in 2nd half of 1983