Schedule for the 21st Design Automation Conference, Albuquerque, NM

MONDAY, June 25

Session 1

9:00 Keynote address: "Artifacts, Tools, and Infrastructures: New Opportunities for Creating and Propagating Knowledge"
Speaker: Lynn Conway, Defense Advanced Research Projects Agency

Session 2-Kh'a

Simulation-Recent Developments
Chairperson: L. Rosenberg, RCA Corp.

1:30 (2.1) "An Experimental MaS Fault Simulation Program CSASIM," J.P. Hayes, M. Kawai, University of Michigan
(2.2) "The Second Generation MaTIS Mixed-Mode Simulator," e.F. Chen, CoY Lo, H.N. Nham, AT&T Bell Laboratories
(2.3) "Stafan: An Alternative to Fault Simulation," S.K. Jain, V.D. Agrawal, AT&T Bell Laboratories
(2.4) "Themis: A Mix Mode, Multi-Level, Hierarchical Interactive Circuit Simulator," M.H. Doshi, R. Sullivan, D. Schuler, Prime Computer, Inc.

Session 3-Room A

Routing Algorithms
Chairperson: K. Roberts, UTMC

1:30 (3.1) "A Two-Dimensional Channel Router for Cell Arrays," G.R. Dupenloup, IMAG, France
(3.2)"An Efficient Channel Router," T Yoshimura, NEC Corp., Japan
(3.3) "A Global Routing Algorithm for General Cells," G.W Clow, M.I.T
(3.4) "A Symbolic Interconnect Router for Custom IC Design," e.H. Ng, VLSI Technology, Inc.

Session 4-Room B

Hardware Description Languages
Chairperson: e. Rose, Case Western University

1:30 (4.1) "Harpn A Hierarchical Multi-Level Hardware Description Language," P.M.B. Veiga, MJ.A. Lanca, Technical University of Lisbon, Portugal
(4.2) "ADL: An Algorithmic Design Language for Integrated Circuit Synthesis," W.H. Evans, J.e. Ballegeer, N.H. Duyet, Thomson-CSF, France
(4.3) "A Symbolic Functional Description Language," G. Odawara, J. Sato, M. Tomita, University of Tokyo, Japan
(4.4) "Block Description Language (BDL) Structural Description Language," E. Slutz, G. Okita, J. Wiseman, Hewlett-Packard

Session 5-Cochiri

Workshop: Silicon Compilers and Expert Systems for VLSI (Admission by ticket only)
Moderator: D. Gajski, University of Illinois

1:30 Panelists: H. Brown, Stanford University; D. Johannsen, Silicon Compilers, Inc.; J. Southard, Metalogic, Inc.; D. Thomas, Carnegie-Mellon University; L. Steinberg, Rutgers University; M. Buric, Silicon Design Lab, Inc.

Session 6-Sandia

Workshop: Introduction to Gate-Array Placement and Routing Packages
(Admission by ticket only)
Moderator: F Hinchliffe, Sanders Associates, Inc.

1:30 Panelists: R.V. Alessi, Eastman Kodak Co.; J. Runik, California Devices, Inc.; P. Catapano, Jr., Raytheon Co.; M. Kubota, Digital Equipment Corp.; R.H. Dean, Trilogy Systems Corp.; E. Dorsey, Automated Design Engineering; M. Leddell, Honeywell, Inc.

Session 7-Kiva

Module Generators
Chairperson: Neil Weste, AT&T Bell Laboratories

4:00 (7.1) "Technology Independent MaS Multiplier Generator," K-C Chu, R. Sharma, AT&T Bell Laboratories
(7.2) "The Icewater Language and Interpreter," P.A.D. Powell, I. Elmasry, University of Waterloo, Canada
(7.3) "Cell Compilation with Constraints," e. Lursinsap, D. Gajski, University of Illinois

Sessions 8-Room A

CAD Data Base Systems
Chairperson: FW Day, AT&T Bell Laboratories

4:00 (8.1) "Efficient Implementation of Experimental Design Systems," G.D.M. Ross, University of Edinburgh, Scotland
(8.2) "Extending Relational Data Model for Design Applications," M. Hardwick, Texas Tech University
(8.3) "The Structure and Operation of a Relational Data Base System in a Cell-Oriented Integrated Circuit Design Syslem," L.A. Hollaar, TM. Carter, B.E. Nelson, R.A. Lorie, University of Utah

Session 9-Room B

Layout Improvements
Chairperson: L. Abel, Applieon, Inc.

4:00 (9.1) "Hierarchical Error-Tolerant Compaction," e. Kingsley, VLSI Technology, Inc.
(9.2) "Chip Layout Optimization Using Critical Path Weighting," A.E. Dunlop, V.D. Agrawal, D.N. Deutsch, M.F Jukl, P. Kozak, M. Wiesel, AT&T Bell Laboratories
(9.3) "Interactive Compaction Router for VLSI Layout," H. Mori, Nippon Electric Co., LId., Japan

Session IO-Room C

Basic Thtorial: Logic Programming for Digital System CAD

4:00 Speakers: E.P. Stabler, Syracuse University; P.W. Horslmann, IBM Corp.

TUESDAY, June 26

Session II-Kiva

Magic: A VLSI Layout System
Chairperson: J.K. Ousterhout, University of California (Berkeley)

8:00 (11.1) "Magic: A VLSI Layout System," J.R. Ousterhout, G.T Hamachi, R.N. Mayo, WS. Seoll, G.S. Taylor, University of California (Berkeley)
(11.2) "Magic's Incremental Design-Rule Checker," G.S. Taylor, J.K. Ousterhout, University of California (Berkeley)
(11.3) "Plowing: Interactive Stretching and Compaction in Magic," W.S. Scott, J.K. Ousterhout, University of California (Berkeley)
(11.4) "A Switchbox Router with Obstacle Avoidance," G.T Hamachi, J.K. Ousterhout, University of California (Berkeley)

Session 12-Room A

Test Algorithm Refinements
Chairperson: E. Ulrich, Digital Equipment Corp.

8:00 (12.1) "Test Generation for LSI: A Case Study," H.K. Reghbati, M.S. Abadir, Simon Fraser University, Canada
(12.2) "A Practical Approach to Testing Microprocessors," M.G. Karpovsky, R.G. Van Meter, Boslon University
(12.3) "Chip Partitioning Aid: A Design Technique for Partitionability and Testability in VLSI," S. DasGupta, M.e., Grar., R.A. Rasmussen, R.G. Walther, TW Williams, IBM Corp.
(12.4) "An Integrated Design for Testability and Automatic Test Pattern Generation System: An Overview," E. Trischler, Siemens Corporation Research and Support, Inc.

Session I3-RoOln B

Panel: The SRC Design Sciences Research Program (University Industrial Research Cooperation in ICiCAD)
Moderator: R.K. Cavin, Semiconductor Research Corp.

8:00 Panelists: S.W Director, Carnegie-Mellon University; D. Pederson, University of Califomia (Berkeley); J. Daughton, Honeywell, Inc.

Session /4-Room C

Basic Tutorial: Layout Tools-What Really is There
8:00 Speaker: R. Smith, Star Technologies, Inc.

Session 15-Room C

Invited Paper: "Ergonomic Studies in Computer-Aided Design"
9:00 Speaker: G.H. van der Heiden, Swiss Federal Institute of Technology, Switzerland

Session /6-Kh'a

Layout Verification and Design-Rule Checking
Chairperson: D. Coelho, Silvar-Lisco

10:30 (16.1) "Function Verification of Memory Circuits from Mask Artwork Data," M. Kawamura, H. Takagi, K. Hirabayashi, Toshiba Corp., Japan
(16.2) "Scanline Approach to Design Rule Checking: Computational Experience," P.T. Chapman, K. Clark, Jr., IBM Corp.
(16.3) "A Systolic Design Rule Checker," R. Kane, S. Sahni, University of Minnesota

Session 17~Room A

Functional Simulation and Analysis
Chairperson: P. Goel, AIDS, Inc.

10:30 (17. I) "A Model for Hardware Description and Verification," GJ. Milne, University of Edinburgh, Scotland
(17.2) "A Functional Hardware Description Model and Its Simulator," R. Alali, Universit', des Sciences et Techniques du Languedoc, France
(17.3) "Toward A Standard Hardware Description Language," KJ. Lieberherr, GTE Laboratories, Inc.

Session 18-Room B

Design Tools and Interfaces
Chairperson: M. d'Abreu, Phoenix Data Systems, Inc.

10:30 (18.1) "IGES as an Interchange Format for Integrated Circuit Design," e.H. Parks, General Dynamics
(18.2) "A Designing System for Multifamily Housing," B. Jackson, New Jersey Institute of Technology
(18.3) "Module Design Verification System MDVS," L.H. Wilkins, IBM Corp.

Session 19-Room C

Human Factor and Engineering Workstations
Chairperson: FS. Frome, AT&T Bell Laboratories

10:30 (19.1) "Studying the Mouse for CAD Systems," L. Price, Calma Co.
(19.2) "AMOEBA: A Symbolic VLSI Layout System," R. Goldin, B. Juran, Honeywell, Inc.
(19.3) "ARIES: A Workstation-based, Schematic Driven System for Circuit Design," W.H. Kao, M.H. Movahed-Ezazi, M.L., Sabiers, Xerox Corp.

Continued

Session 20-Kivo
Synthesis
Chairperson: A. Goldfein, Phoenix Data Systems
1:30 (20.1) "A High-Level Synthesis Tool for MOS Chip Design," J. Dussault., C-c.. Liaw., M. Tong, AT&T Bell Laboratories
(20.2) "Emerald: A Bus-Style Designer," C-J. Tseng, Carnegie Mellon University
(20.3) "Polaris: Polarity Propagation Algorithm for Logic Synthesis," T. Shinsha, T Kubo, M. Hikosaka, K. Akiyama, K. Ishihara, Hiyachi, Ltd., Japan
(20.4) "A General Methodology for Synthesis and Verification of Register-Transfer Designs"," A.C.. Parker, F. Kurdahi, M. Mlinar. University of Southern California

Session 2/-Room A
Topics in Simulation
Chairperson: P. Drongowski. Case-Western Reserve University
1:30 (21.1) "The Ultimate Simulation Engine," M.E. Glazier, A.P.. Ambler, University of Manchcstcr, England
(21.2) "ORACLE: A Simulator for Bipolar and MOS IC Design," M.A. d'Abreu, K.L.. Cheong, TC.. Flanagan. Honeywell Corp.
(21.3) "A Multiprocessor Implementation of Relaxation-Based Electrical Circuit Simulation.", J.T.. Deutsch. A.R. Newton., University of Calif ornia (Berkcicy)
(21.4) "Micro-Computer Oriented Algorithms for Delay Evaluation of MOS Gates,"," D. Etiemble, V. Adeline. N.H. Duyet., J.e.. Balleger., Universite P. et M. Curie. France

Session 22-Room B
AT&T Bell Labs CAD System
Chairperson: S. Pardee, AT&T Bell Laboratories
1:30 (22.1) "A Unified CAD System for Electronic Design,"," J.e.. Foster. AT&T Bell Laboratories
(22.2) "Engincering Design Aspccts.", H. Y Chang, AT&T Bell Laboratories
(22.3) "Physical Design Aspects,"," C.W. Rosenthal., AT&T Bell Laboratories
(22.4) "Users View,"" J.R. Colton., F.E. Swiatek. AT&T Bell Laboratorics: D.H. Edwards., AT&T Technologies

Session 2J-Cochili
Workshop: The Semicustom Revolution: How to Thrive or Survive (Admission by ticket only)
Moderator: T Zingale. Daisy Systems Corp.
I:30 Panelists: F. Kohn, Mentor Graphics Corp.: F Lynch. Valid Logic Systems. Inc.: D. Kulbarsh. Silvar-Lisco

Session 24-Sandia
Workshop: Introduction to Gate-Array Placement and Routing Packages (Admission by ticket only)
I:30 Moderator: F. Hinchliffe. Sanders Associates
(Note: This a'orks/wp is idemica/IO Session 6.)

Ses.l';Oll 25-Kh'1l
Automatic Placement
Chairperson: H.E. Krohn. Zycad Corp.
4:00 (25. I) "The Channel Expansion Problem in Hicrarchical Layout Design," R.R. Chen., San Jose State University.
(25.2) "A Standard-Cell Initial Placemcnt Stratcgy." B.D. Richard., Sandia National Laboratories
(25.3) "Performancc of Algorithms for Constructive Initial Placement.", M. Palczcwski. Metheus Corp.

Session 26-Root1l A
Rutger Artificial Intelligence VLSI CAD
Chairperson: D. Thomas. Carnegic-Mellon University
4:00 (26. I) "Gcncralization of SymbOlic Layout.", J.A. Roach. Rutgcrs Univcrsity
(26.2) "A Knowlcdge-Based Approach to VLSI CAD," L.I.. Steinberg, TM. Mitchell, Rutgers University
(26.3) "Critter System Automated Critiquing of Digital Hardware Systems," V.E. Kelly, Rutgers University

Session 27-Room B
PLA Design Techniques
Chairperson: G.B. Goates, CAE Systems, Inc.
4:00 (27.1) "A Branch and Bound Algorithm for Optimal PLA Folding," J.L.. Lewandowski, C.L.. Liu, University of Illinois
(27.2) "A VLSI FSM Design System," M.J. Meyer, P. Agrawal., R.G. Pfister, AT&T Bell Laboratories
(27.3) "The Semi-Automatic Generation of Processing Element Control Paths for Highly Parallel Machines.", T.M. Sabaty, B. Mathies. D.E. Shaw, Columbia University

Session 28-Room C
CAM/CAT Applications
Chairperson: 1. Miller, Honeywell, Inc.
4:00 (28.1) "Managing a Large Volume of UniqU<; Part Numbers in a Semiconductor Factory,"," V.J. Freund, Jr.., IBM Corp.
(28.2) "An Advanced Proximity Correction Technique for the IBM EL-2 Electron Beam Tool," W. J. Guillaume. A. Kurylo, IBM Corp.
(28.3) "An Automated System for Testing LSI Memory Chips.", H.D. Schnurmann. L.J.. Vidunas., R.M. Peters. IBM Corp.

WEDNESDAY, June 27

Session 29-Ki\{1
Intel Design Automation System
Chairperson: J. Owen., Intel Corp.
8:00 (29.1) "The Intel Design Automation System,"," S. Nachtsheim, Intel Corp.
(29.2) "The Engineering Design Equipment,"," K. Sherhart. J. Owen., Intel Corp.
(29.3) "Functional Design Verification by Multi-Level Simulation,"," K. Tham., D. Wimp., R. Willoner., Intel Corp.
(29.4) "Perfonnance Verification of Circuits,"," J. Mar., Y-P. Wei, Intel Corp.
(29.5) "Hierarchical Layout Verification,"," TJ. Wagner., Intel Corp.

Se.l:.I'iolB0-Room A
Testing Problems and Solutions
Chairperson: J. Arabian, Digital Equipment Corp.
8:00 (30. I) "Taking into Account Asynchronous Signals in Functional Test of Complex Circuits,"," C. Bellon., R. Velazco. Institut Imag. France
(30.2) "VLSI Test Expertise System Using a Control Flow Model,"," G. Saucier. C. Bellon., Institut Imag., France
(30.3) "A Gate-Level Model for CMOS Combinational Logic Circuits with Application to Fault. Detection,"," S.M. Reddy. University of Iowa: V.D. Agrawal., AT&T Bell Laboratories
d0.4) "Parameterized Random Testing.","," KJ. Lieberherr. GTE Laboratories. Inc.

Session 3/-Roum 8
Advanced Tutorial: Functional Testing Techniques for Digital LSI/VLSI Systems
8:00 Speaker: S. Y.H. Suo State University or New York

SeJJ;OlI 32~Roo", C
Timing Analysis
Chairperson: D.R. Tryon., IBM Corp.
8:00 (32.1) "Delay and Power Optimization in VLSI Circuits,"," L.A. Glasser., L.P.J. Hoyte. M.I.T
(32.2) "IDA: Interconnect Delay Analyzer for ICs.," A.J. de Geus. J.B. Reed. *M.I.*, Rekhson. G. Wikle., General Electric Microelectronics Center
(32.3) "Switch-Level Delay Models for Digital MOS VLSI.","," J.K. Ousterhoul., University of California (Berkeley)
(32.4) "An MOS Digital Network Model Based on a Modified Thevenin Equivalent for Logic Simulation," T Takahashi, S. Kojima, O. Yamashiro, K. Eguchi, H. Fukuda. Musashi Works of Hitachi Ltd., Japan

Sessiolk 33-Room B
Panel: The VHSIC Hardware Description Language (VHDL) Program
Moderator: Al Dewey, AFWAUAADE. Wright-Patterson AFB
9:00 Panelists: J. Hines. AFWALIAARM, Wright-Patterson AFB; J. Hanne, Microelectronics & Computer Technology Corp.: H. Cloud, IBM Corp .., Federal Systems Division; A. Lowenstein. Prospective Computer Analysts. Inc.

Session 34-Kiva
Layout Systems
Chairperson: C. McCaw. IBM Corp.
10:30 (34.1) "CAESAR 45: An Enhanced Version of CAESAR Supporting 45° Geometries.", A. Lanfri. Metheus Corp.
(34.2) "MICON: A Knowledge-Based Single Board Computer Designer." W. P. Birmingham., D.P. Siewiorek., Carnegie-Mellon University
(34.3) "MGX: An Integrated Symbolic Layout System for VLSI,"," M. Ozaki., M. Watanabe., M. Ikeda. M. Kakinuma. K. Sato. Mitsubishi Electric Corp .., Japan

5C',55;01/ 35-Room A
Integrated Circuit Design s)stems
Chairperson: YE. Lien. AT&T Bell Laboratories
10:30 (35.1) "UTMCs LSI CAD System-HIGHLAND,"," K. Anderson. R. Powell., United Technologies Microelectronics Center
(35.2) "Mimola Design System: Design Tools of Digital Processors,"," P. Marwedel., University or Kiel. West Germany
(35.3) "A Declarative Design Approach for Combining Macro Cells by Directed Placement and Constructive Routing,"," C. Wardle. C. Watson. C. Wilson. C. Mudge. B. Nelson. Commonwealth Scientific & Industrial Research Organization. Australia

Session 36-Room B
Panel: A Model for University/Industry/Government Cooperation
Moderator: L. Snyder. University of Washington
10:30 Panelists: W.1. Hcnry. Boeing Aerospace Co .; H. Kocman. University of Washington: R.W. Ritchie. Xerox Corp.: P.R. Young. University Of Washington

Session 37-Room C
Tutoral: Mechanical Workstation Software
"Computer-Aided Engineering in the Mechanical Design Process"
10:30 Speaker: 1. SCOll. GE-CAE International

Session 38-Room C
lutorial: Mechanical Engineering Hardware
"Direction in Workstation Technology"
11:15 Speaker: R. Nadeau. Computervision

Session 39-Ki\'(1
Layout Extraction
Chairperson: K. Wu. AT&T Bell Laboratories
2:00 (39.1) "Technology Independent Btock Extraction Algorithm.", F. Luellau., T Hoepken. E. Barke. Univcrsitul Hannover. West Germany
(39.2) "ExcleA Circuit Extractor for TC Designs.","," S.P. McCormick. M.I.T
(39.3) "An Interactive Electrical Graph Extractor,"," J.L. Kors. M. Israel., Institut d'Infonnatique d'Entreprise. France

Se.l:.I'iol40-Roolll A
Artificial Intelligence and Geometric Data Bases
Chairperson: S. Y Levy. Rutgers University

Continued

2:00 (40.1) "Some Consideration of the Data Model of Geometric Data Bases," J. Zhang, R. Wang, Beijing Institute of Aeronautics and Astronautics, The People's Republic of China

(40.2) "An Architecture for Application of AI to Design." J.R. Dixon. M.K. Simmons, General Electric Corp.; P.R. Cohen, University of Massachusetts

(40.3) "A Formal Design Verification System Based on an Automated Reasoning System." A.S. Wojcik, J. Kljaich. N. Srinivas. Illinois Institute of Technology

Session 4/-Room B

Panel: Hardware Accelerators vs. General-Purpose Computers

Moderator: R. Banin, Daisy Systems Corp.

2:00 Panelists: D. McCubbrey. Environmental Research Institute of Michigan; J. Kohn, IBM Corp.; T Blank. Stanford University; R. Retberg, Bolt., Bernack, Newton

Session 42-Cochiri

Workshop: The Semicustom Revolution: How to Thrive and Survive (Admission by ticket only)

2:00 Moderator: T Zingale. Daisy Systems Corp. *(Note: This 1V0rkshop is identico/ to Ses.l·ion 23.)*

Session 43-Sondio

Workshop: Silicon Compilers and Expert Systems for VLSI (Admission by ticket only)

2:00 Moderator: D. Gajski, University of Illinois *(Note: This session is identical to Session 5.)*

Session 44-Kiva

Floor Planning Short Papers

Chairperson: W. Heller. IBM Corp.

4:00 (44.1) "Optimization Techniques for Two-Dimensional Placement," L.A. Markov, J.F. Fox, J.H. Blank, GTE Laboratories.

(44.2) "An Algorithm for Finding a Rectangular Dual of a Planar Graph for Use in Area Planning for VLSIIntegrated Circuits.", K. Kozminsk. University of Rochester

(44.3) "Gala-Automatic Layout System for High Density CMOS Gate Arrays." B.N. Tien, B.S. Ting. TO. Cheam. K. Chow, S.c. Evans. Hughes Aircraft. Co.

(44A) "Algorithm for Building Rectangular Floor-Plans," S.M. Leinwand. Y-T Lai, University of Illinois

(44.5) "Spider: A Chip Planner for ISL Technology," P. Rao. R. Ramnarayan, Honeywell Corp.; G. Zimmerman, Univcrsitat Kaiserslautern, West Gernlany

(44.6) "Combine and Top-Down Block Placement Algorithm for Hierarchical Logic VLSI Layout." T Kozawa, C. Mirura, H. Terai, Hitachi LId., Japan

Session 45-Room A

Layout Short Papers

Chairperson: D. Lambert. IBM Corp.

4:00 (45.1) "Initial Placement of Gate Arrays Using Least-Squares Methods." J. P. Blanks, VR Information Systems. Inc..

(45.2) "Module Positioning Algorithms for Rectilinear Macrocell Assemblies." J.A. Hudson, J.A. Wisniewski, Sandia National Laboratories~ R.C.. Peters, Kirk-Mayer. Inc.

(45.3) "Compiling Random Logic Finite State Controllers," E. Ronald. Cambridge University. England

(45.4) "Microprocessor Synthesis," B.M. Pangrle, V.K. Raj, D.O. Gajski, University of illinois

(45.5) "Topological Routing of Multi-Bit Data Buses," G. Persky, L. V. Tran. Hughes Aircraft Co.

Session 46-Room B

Design Methods Short Papers

Chairperson: 1. Crabbe. RCA Corp.

4:00 (46.1) "An Electronic Design Interchange Format." J.D. Crawford. Tectronix. Inc.

(46.2) "A VLSI Design Methodology Based on Parametric Macro Cells." R.A. Kriete. R.K. Nettleton. Harris Corp.

(46.3) "Methodology for Compiler Generated Silicon Structures," A. Martinez, S. Nance. R. Duyn, VLSI Technology, Inc.

(46A) "Design Transaction Management.", R.H. Katz, University of California (Berkeley): S. Weiss, University of Wisconsin-Madison

(46.5) "Uniform Support for Information Handling and Problem Solving Required by the VLSI Design Process.", V. Ashok. W. McKnight., J. Ramanathan, Ohio State University

(46.6) "VTI Compose-Powerful Graphical Chip Assembly Tooi.;' S. Trimberger., VLSI Technology. Inc.

Session 47-Room C

Analysis/Optimization Short Papers

Chairperson: Y. Agrawal. AT&T Bell Laboratories

4:00 (47.1) "Computer-Aided Minimization Procedure for Boolean Functions," N.N. Biswas. Indian Institute of Science. India

(47.2) "Optimization of Negative Gate Networks Realized in Weinberger-Like Layout in a Boolean-level Silicon Compiler.", M. Perkowski, A. Wieclawski, Portland State University

(47.3) "Deadlock Analysis in the Design of Data-Flow Curcuits." C.S. Jhon, University of Iowa

(47A) "A Method for IC Layout Verification," O.A. Marvik. University of Trondheim. Norway

(47.5) "On the Relation Between Wire Length Distributions and Placement of Logic on Master Slice ICs," A.C.. Parker. F. Kurdahi. M. Mlinar, University of Southern California D