Session 20-Kiv, Synthesis
1:30 (20.1) "A High-Level Design Methodology for MOS Chip Design," J. Dussault, C.-c. Liu, M. Tong, AT&T Bell Laboratories
(20.2) "Emerald: A Bus-Style Designer," C.J. Teng, Carnegie Mellon University
(20.4) "A General Methodology for Synthesis and Verification of Register-Transfer Designs," A.C. Parker, F. Karulaki, M. Milor, University of Southern California

Session 25-Room A, Topics in Simulation
Chairperson: P. Duongson, Case-Western Reserve University
1:30 (25.1) "The Ultimate Simulation Engine," M.E. Glueck, A.P. Ambler, University of Manchester, England
(25.4) "Micro-Computer Oriented Algorithms, for Delay Evaluation of MOS Gates," D. Ehrenfeld, V. Adeline, N.H. Duyer, J.e. Rolfege, University, P. et M. Curt, France

Session 22-Room B, AT&T Bell Labs CAD System
Chairperson: S. Padro, AT&T Bell Laboratories
1:30 (22.1) "A Unified CAD System for Electronic Design," I.e. Foster, AT&T Bell Laboratories
(22.2) "Engineering Design Aspects," H.Y. Chang, AT&T Bell Laboratories
(22.3) "Physical Design Aspects," C.W. Rosen-Chang, AT&T Bell Laboratories
(22.4) "Users’ View," J.R. Colton, F.E. Swiatek. J.R. Colton, F.E. Swiatek.

Session 20-Room B, Case Studies in Symbolic Layout
Chairperson: G.B. Goates, CAE Systems, Inc.
4:00 (20.1) "A Branch and Bound Algorithm for Optimal PLA Folding," J.J. Lwowski, C-L. Liu, University of Illinois
(20.2) "A VLSI FSM Design System," M.J. Meyer. P. Agrawal, R.G. Pfeifer. AT&T Bell Laboratories

Session 27-Room B, PLA Design Techniques
4:00 (27.1) "Managing a Large Volume of Unicp: Part Numbers in a Semiconductor Factory," V.J. Freund. Jon Fag. IBM Corp.
(27.2) "A Method for Elimination of Proximity Correction Technique for the IBM EL-2 Elagton Beam Tool," V. J. Guillaume, A Kurylo. IBM Corp.
(27.3) "An Automated System for Testing LSI Memory Chips," H.D. Schuman, J.L. Vidonas, R.M. Petersen. IBM Corp.

Session 25-Room A, Advanced Tutorial: Gate Array Placement and Routing Packages
Chairperson: J. Owen, Intel Corp.
8:00 (25.1) "The Intel Design Automation System," S. Nachtmann. Intel Corp.
(25.3) "Functional Verification by Multi-Level Simulation," K. Tham, D. Wimp, R. Wilkel. Intel Corp.
(25.4) "Performance Verification of Circuits," J. Mar, Y.P. Wei. Intel Corp.
(25.5) "Hierarchical Layout Verification," T.J. Wagner. Intel Corp.

Session 37-Room A, Testing Problems and Solutions
Chairperson: J. Arabia, Digital Equipment Corp.
8:00 (37.1) "Taking into Account Asynchronous Signals in Functional Test of Complex Circuits," C. Bellon, R. Velasco, Instytut Automatyzacji, France
(37.2) "VLSI Test Expertise System Using a Control Flow Model," G. Sancier, C. Bellon, Institut Automatyzacji, France
(37.3) "A Gate-Level Model for CMOS Combinational Logic Circuits with Application to Fault Detection," S.M. Reddy. University of Iowa. V.D. Agrawal. AT&T Bell Laboratories

Chairperson: S.Y.H. Sue State University of New York
8:00 Speaker: S.Y.H. Sue State University of New York

Session 32-Room C, Artificial Intelligence and Geometric Data Bases
Chairperson: S.Y.Levy. Rutgers University

Session 33-Room B, Panel: The VHDL Hardware Description Language (VHDL) Program
Chairperson: Al Dewey, APWAAADE. Wright-Patterson AFB
9:00 Panelsco: J. Hines. APWAAADE. Wright-Patterson AFB

Session 34-Room A, Layout Systems
Chairperson: C. McCaw. IBM Corp.
(34.3) "Domain Specific CAD Systems: A Case Study," B.D. Widener, AFWA, Wright-Patterson AFB
11:15 Speaker: R. Nadeau. Computervision Corporation

Session 36-Room B, Integrated Circuit Design System
Chairperson: R. Esten. Lien. AT&T Bell Laboratories
10:30 (36.1) "UTMICS: LSI CAD Systems," K. Anderson, R. Powell, United Technologies Microelectronics Center
(36.2) "Multifunction Design System Design Tools of Digital Processors," P. Marwedel. University, or K. West Germany

Session 38-Room C, Tutorial: Mechanical Engineering Hardware
Chairperson: R. Nadeau. Computervision Corporation
10:30 Speaker: S. COHL, GE. CAE. International

Session 39-Room A, Layout Extraction
Chairperson: K. Wu. AT&T Bell Laboratories
2:00 (39.1) "Technology Independent Block Extraction Algorithm," F. Luellau, T. Hoepken, E. Barke, J. Hulsmann, IBM Corp.
(39.3) "An Interactive Electrical Graph Extractor," J.L. Kors. M. Israel. Institut d’Informatique & d’Automatique, France

Session 36-Room B, Artificial Intelligence and Geometric Data Bases
Chairperson: S.Y.Levy. Rutgers University
11:15 Speaker: R. Nadeau. Computervision Corporation

Session 34-Room A, Artificial Intelligence and Geometric Data Bases
Chairperson: S.Y.Levy. Rutgers University
Session 44: Kiva
Session 43: Sondio
Session 42: Cochiri

2:00 (44.1) "Some Consideration of the Data Model of Geometric Data Bases," J. Zhang, R. Wang, Beijing Institute of Aeronautics and Astronautics, The People's Republic of China

2:00 (44.2) "An Algorithm for Finding a Rectangular Dual of a Planar Graph for Use in Area Planning for VLSI Integrated Circuits," K. Kozminski, University of Rochester

2:00 (44.3) "Gala: Automatic Layout System for High Density CMOS Gate Arrays," B.N. Tien, B.S. Ting, TO. Cheam, K. Chow, S.C. Evans, Hughes Aircraft Co.

2:00 (44A) "Algorithms for Building Rectangular Floor Plans," S.M. Leinwand, Y-T Lai, University of Illinois

2:00 (44.5) "Spider: A Chip Planner for ISL Technology," P. Rao, R. Ramnarayan, Honeywell Corp.; R. Retberg, Bolt, Beranek, and Newman, Inc.

2:00 (44.6) "Combine and Top-Down Block Placement Algorithm for Hierarchical Logic VLSI Layout," T. Kozawa, C. Mirura, H. Terai, Hitachi Ltd., Japan

2:00 Panelists: D. McCubbrey, Environmental Research Institute of Michigan, J. Kohn, IBM Corp.; T. Blank, Stanford University; R. Retberg, Bolt, Beranek, and Newman, Inc.

Chairperson: W. Heller, IBM Corp.

Session 45: Room B
Panel: Hardware Accelerators vs. General-Purpose Computers
Moderator: R. Bain, Daisy Systems Corp.

2:00 Workshop: The Semicustom Revolution: How to Thrive and Survive (Admission by ticket only)
Moderator: T. Zingale, Daisy Systems Corp.
(Note: This workshop is identical to Session 23.)

2:00 Session 45: Sondio
Workshop: Silicon Compilers and Expert Systems for VLSI (Admission by ticket only)
Moderator: D. Gajski, University of Illinois
(Note: This session is identical to Session 5.)

Floor Planning Short Papers
Chairperson: W. Heller, IBM Corp.

4:00 (45.1) "Initial Placement of Gate Arrays Using Least-Squares Methods," J.P. Blanks, V.R. Information Systems, Inc.

4:00 (45.2) "Module Positioning Algorithms for Rectilinear Macrocell Assemblies," J.A. Hudson, J.A. Winstead, Sandia National Laboratories;

4:00 (45.3) "Combing Random Logic Finite State Controllers," E. Ronald, Cambridge University, England

4:00 (45.4) "Microprocessor Synthesis," B.M. Pangle, V.K. Raj, D.O. Gajski, University of Illinois

4:00 (45.5) "Topological Routing of Multi-Bit Data Buses," G. Persky, L.V. Tran, Hughes Aircraft Co.

Session 46: Room B
Design Methods Short Papers
Chairperson: J. Crabbe, RCA Corp.

4:00 (46.1) "An Electronic Design Interchange Format," J.D. Crawford, Tectronix, Inc.

4:00 (46A) "Design Transaction Management," R.H. Katz, University of California (Berkeley); S. Weiss, University of Wisconsin-Madison

4:00 (46.2) "A VLSI Design Methodology Based on Parametric Macro Cells," R.A. Kriete, R.K. Nedelton, Harris Corp.

4:00 (46.3) "Methodology for Compiler Generated Silicon Structures," A. Martinez, S. Nance, R. Ramnarayan, Honeywell Corp.; R. Retberg, Bolt, Beranek, and Newman, Inc.

4:00 (46.4) "Algorithm for Building Rectangular Floor Plans," S.M. Leinwand, Y-T Lai, University of Illinois

4:00 (46.5) "Designs and Systems for VLSI Integrated Circuits," K. Kozminski, University of Rochester

4:00 (46.6) "VTI Compose-Powerful Graphical Chip Assembly Tool," S. Stembo, VLSI Technology, Inc.

Session 47: Room C
Analysis/Optimization Short Papers
Chairperson: V. Agrawal, AT&T Bell Laboratories

4:00 (47.1) "Computer-Aided Minimization Procedure for Boolean Functions," N.N. Biswas, Indian Institute of Science, India

4:00 (47.2) "Optimization of Negative Gate Networks Realized in Weinberger-Like Layout in a Boolean-Level Silicon Compiler," M. Perkowski, A. Wieczorek, Portland State University

4:00 (47.3) "Deadlock Analysis in the Design of Data-Flow Controllers," C. Bon, University of Iowa

4:00 (47.4) "A Method for IC Layout Verification," O.A. Marvik, University of Trondheim, Norway

4:00 (47.5) "Diodes and Transistors—Placement and Routing of Logic on Master Slices," A.C. Parker, F. Kondili, M. Milner, University of Southern California

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