A Survey of Silicon Foundries

Company, person to contact.	Code	Technologies Available (Minimum feature sizes are also shown.) nMOS me-g	nMOS si-g	pMOS me-g	pMOS si-g	CMOS me-g	CMOS si-g	Bipolar	Preferred Data Format
Acrian Inc. 10131 Bubb Road Cupertino, CA 95014 (408) 996-8522 Jim Huiskens or Jed Rice	AC	x						x	Working plates.
American Microsystems, Inc. (A Division of Gould, Inc.) 3800 Homestead Road Santa Clara, CA 95051 (408) 246-0330 Steve McMinn, Customer Design Engineering Manager	AM		x 5 to 6μm, 4μm, 3μm	x 6 to 7.5μm	x 6μm		7.5μm, 5μm, 5μm Iso-CMOS, 3μm Iso-CMOS		Database tape, PG tape, masks.
ASEA HAFO U.S. Sales Office 66 Bovet Road San Mateo, CA 94402 (415) 574-5400 Anders Dejenfelt, U.S. Sales Manager	AH					x CMOS/bulk 5μm	x CMOS/SOS 4μm		CIF, Calma, Applicon or other database tape format, with circuit information only. (Scribe lines, PCMs, etc. are inserted by ASEA HAFO.) PG tapes also accepted.
CSI Technology Services (Comdial Semiconductor, Inc.) 1230 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-1800 Gary P. Kennedy, Vice President/Operations	CS		x 5μm, 3½ to 5μm Iso-nMOS				x 6μm, 4 to 5μm Iso-CMOS		Masks, database tapes (including CIF), PG tapes
Cherry Semiconductor Corp. 2000 South County Trail East Greenwich, RI 02818 (401) 885-3600 David R. Pryce Marketing Manager	CH							x I^2L, bipolar linear, opto-electronic	Scaled drawings, database tape (Calma or Applicon), photomasks.
Dionics 65 Rushmore Street Westbury, NY 11590 (516) 997-7474 B. Kravits President	DI							x 8μm min. dimensions, dielectrically isolated	Masks.
EXAR Integrated Systems, Inc. 750 Palomar Avenue Sunnyvale, CA 94088 (408) 732-7970 Thruston Awalt, Senior Applications Engineer	EX					x 8μm	x 6μm	x Linear, I^2L	Masks, PG tapes, data base tapes (prefers Applicon format
Four-Phase Systems, Inc. (A Subsidiary of Motorola, Inc.) 10700 North De Anza Blvd. Cupertino, CA 95014 (408) 255-0900 Donald D. Whitman Materials Manager, Semiconductor Operations	FP	x 7μm	x 5μm	x 9μm		x 7μm	x 5μm		Masks.

*me-g = metal-gate
si-g = silicon-gate

[For further details about a particular foundry's services, circle the appropriate letter code (shown in the second column of the survey) on the READER SERVICE card.]

Minimum Production Run	Turnaround Time	Process Control Monitor	Special Capabilities or Considerations
20 to 25 3" diameter wafers.	4 to 6 weeks is typical (3 weeks in "emergencies.")	Information not available.	Prefers to involve its own engineers in the design early, to ensure that the design conforms to its standard processes. Acrian primarily manufactures RF and microwave devices, but also offers foundry services.
"Development orders": 5-wafer minimum. Annual production requirements under 5000 parts.	PG tape to packaged prototypes: 7 to 12 weeks. Masks to packaged prototypes: 5 to 8 weeks.	Can be supplied either by foundry or by customer. (Foundry prefers to step its own PCM's into production masks.)	AMI has manufactured over 850 COT products since 1974, and offers one of the widest selections of technologies and designer-foundry interfaces. AMI subdivides the development cycle into 3 "phases" (see *Semiconductor Manufacturing Considerations for VLSI Designers*, in this issue).
40 3" wafers (bulk). 20 3" wafers (CMOS/SOS).	Database file (received in Sweden) to packaged, tested prototypes: 4 to 6 weeks: CMOS/bulk, 5 to 7 weeks: CMOS/SOS. In special cases, from database file to PCM-tested wafers: 3 to 5 weeks: CMOS/bulk 4 to 6 weeks: CMOS/SOS.	Supplied by foundry.	ASEA HAFO, a $4-billion company, with headquarters and processing facilities in Sweden, is one of the few foundries offering CMOS/SOS.
10 4" diameter wafer starts.	From customer-supplied photoplates to PCM-tested wafers out: 5, 10, or 15 working days (5-μm thick-field n-channel), 10 or 15 working days (6-μm thick-field CMOS and 5-μm Iso n-channel), 15, 20, or 25 working days (5-μm Iso-CMOS).	Supplied either by foundry or by customer.	CSI specializes in very fast turnaround for small-volume customers, and acts as a "prime contractor" for arranging CIF tape conversions, for photomasks, etc. Ion implantation is contracted to IICO (Santa Clara, CA).
Production run: 100 wafers (minimum)	8 weeks (typical): Design-rule check: 1 wk. Mask generation: 2 wks. Wafer fab: 5 weeks.	Supplied by foundry.	Cherry recommends that outside designers review design rules, circuit techniques, and process requirements with them *prior* to mask design.
No wafer-count minimum; rather, a minimum of $10,000 per run.	Information not available.	Information not available.	Dionics manufactures high-voltage display drivers and speciality high-frequency ($f_T \approx 1$GHz) chips. Although the company "doesn't aggressively chase C.O.T. business," it offers a high-performance (high voltage and frequency, low capacitance) process for low-complexity (<100 transistor) devices.
Engineering run: 10 3" wafers (with expectation of production order to follow). Production run: 50 3" wafers.	4 to 12 weeks, depending on processing.	Supplied either by foundry or by customer (preferably by foundry).	A process engineer personally supervises each engineering run.
Production run: 25 wafers (minimum)	Typical process cycle time (masks to PCM-tested wafers): 4 weeks	Supplied either by foundry or by customer.	Formal design rules are available for n-channel silicon-gate, CMOS metal-gate, and p-channel metal-gate processes. Preliminary rules are also available for the Si-gate CMOS process. Four-Phase, primarily a *systems* manufacturer, got into the *semiconductor business* to manufacture proprietary custom chips for its systems. But the internal requirement is small, and excess capacity is devoted to foundry business.

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General Instrument Corp. Microelectronics Division 600 West John Street Hicksville, NY 11802 (516) 733-3000 J. Emyr Edwards Product Marketing Manager	GI		x				x		Database tape (*e.g.*, Calma), masks.
GTE Microcircuits 2000 West 14th Tempe, AZ 85281 (602) 968-4431 Art Gruszynski Product Marketing Manager	GT		x 5μm				x 5μm Iso-CMOS, Iso²-CMOS (2-layer poly)		Calma database tape, PG tapes, masks (Calma database preferred)
Hughes Aircraft Company Solid State Products Division 500 Superior Avenue Newport Beach, CA 92663 (714) 759-2411	HU					x 6μm	x 5μm, 3μm		Calma database tape, PG tape. Masks also accepted (typically for prototype run only).
International Microelectronics Products (IMP) 2830 North First Street San Jose, CA 95134 (408) 262-9100 Shel Schumaker Vice President Marketing	IM				x 3μm		x 3μm Iso-CMOS		PG tapes, database tapes (will also accept masks, but prefers PG or database tape)
Intel Corporation 5000 W. Williamsfield Road Chandler, AZ 85224 (602) 961-2658 Bob Dahlberg, Foundry Marketing Manager	IL		x HMOSI 3.5μm HMOSII 2.0μm				x HCMOS		Database tape (Applicon or Calma).
Intersil, Inc. (A Division of General Electric) 10710 North Tantau Avenue Cupertino, CA 95014 (408) 996-5000 Stephen R. Pollock, Group Product Marketing Manager	IS		x 3μm			x (p-chan. device: 8μm; n-chan. device: 7μm)	x 6μm		Database tape, PG tape.
Micrel, Inc. 1235 Midas Way Sunnyvale, CA 94086 (408) 245-2500 Stan Ericsson, Director Marketing and Sales	MI			x 5μm	x 5μm	x 5μm	x 5μm	x (4-, 8-, and 12-micron epi)	Masks, PG tape, database tape, artwork (will take the job at any point)
Micro-Circuit Engineering, Inc. 1111 Fairfield Drive West Palm Beach, FL 33407 (305) 845-2837	MC					x 6μm		x 20V, 40V linear, I²L, BIFET, BIMOS, Chrome-Silicon	Calma database tape, PG tape, masks.
Mitel Semiconductor Box 13320 Kanata, Ontario Canada K2K 1X5 (613) 592-5630 Gene Cohen	MS						x 5μm, 4μm Iso-CMOS, Iso²-CMOS (2-layer poly)		PG tapes, masks (PG tapes preferred).
Monosil, Inc. 975 Comstock Street Santa Clara, CA 95050 (408) 727-6562 Don Green Sales Manager	MO	x 5μm	x 5μm	x 5μm	x 5μm	x 5μm (Also Iso-CMOS)	x 5μm (Also Iso-CMOS)	x Linear, I²L, high-voltage dielectric-isolation	Masks.

Minimum Production Run	Turnaround Time	Process Control Monitor	Special Capabilities or Considerations
50 wafers (minimum)	10 weeks for prototype parts.	Supplied by foundry.	General Instrument is currently creating a "publishable set of design rules to which a customer may refer to isolate areas of difference or potential design problems, prior to mask/tape submittal."
Prototypes: 15 4" wafers (minimum) Production: 100 4" wafers (minimum) (No required production commitment.)	From PG tapes in to untested wafers out: 8 weeks (typical).	Supplied either by foundry or by customer (preferably by foundry).	GTE Microcircuits uses the term "customer-furnished tooling," or "CFT." A specific group in the production area handles all CFT jobs. Si-gate CMOS process is compatible with Mitel's Iso-CMOS process (GTE is a Mitel licensee). Customers must sign non-disclosure agreements to get GTE Microcircuit's design rules.
Minimum production run: one lot (5 to 10 wafers)	PG tape to packaged (untested) devices: 6 weeks (typical) (less for wafers only).	Supplied either by foundry or by customer (preferably by foundry).	Hughes does 100% ion-implantation (no diffusion), which the company says allows much better process control.
Minimum prototype run: 10 4" diameter wafers out Minimum production run: 250 wafers/month or 10,000 packaged parts/year.	Prototypes: PG in to untested, packaged parts out: 4 weeks (typical). Production: database tape to packaged, tested units out: 10 weeks (typical).	Supplied by foundry.	Will do special packaging (*e.g.*, leadless chip carriers). Will do design-rule-check on database tape (optional). Will provide design and electrical rules after signing non-disclosure agreement.
General minimum: 10,000 devices/year. Looks for business that is commercial, not R&D, in nature.	Database tape to wafers (prototype run): 9 to 12 weeks	Supplied either by foundry or by customer (In any case, Intel's own PCM is always included on the wafer.)	Intel makes certain CAD tools (*i.e.*, in-house circuit simulator, worst-case process files, DRCs) available to foundry customers. In the future, Intel also plans to offer connectivity verification programs. They are clearly in business for *large volume* customers (such as GE and Burroughs) only. Intel says that customers will have access to the "shrink path." (Intel's processes are designed for down-sizing.)
At present, customers must require > 1,000 wafers/year	Database tape in to wafers out: 9 to 10 wks. 1 week for paperwork. 2 weeks to obtain masks. 5 to 6 weeks for wafer fabrication. 1 week for test.	Supplied by foundry.	Intersil prefers to deliver wafers that meet process parameters, rather than probed wafers or tested, packaged customer-designed devices. Si-gate CMOS process provides CMOS UV PROM capability.
Min. production runs: 25 (3" or 4") wafers. Qualification lots: 10 to 20 (3" to 4") wafers	20-working-day "cycle time" (working plates to PCM-tested wafers) for MOS; 30 working days for bipolar.	Supplied by customer.	Formerly a division of Litronix, Micrel has been a privately owned foundry since November. Micrel does a lot of p-channel work and, at added cost, will provide custom process specifications. Micrel has extensive characterization, wafer sort, environmental and final test capability.
No absolute min. run size. Minimum wafer run is generally 100 (4").	Typical turnaround time (masks to finished devices): 12 to 18 weeks (depending on process and on amount of testing required).	Supplied either by foundry or by customer (preferably by customer).	MCE says that it will "work with clients at *any* stage in the design/production cycle." The company will provide fabricated wafers, or fully packaged/tested devices.
Normal minimum run is "several batches" (24 wafers/batch). Will do prototype runs if there is good probability of significant follow-on business.	From masks to wafers: 8 weeks.	Supplied by foundry.	According to a company spokesman, Mitel "does provide some foundry service, but doesn't have much excess capacity." Mitel is not interested in "non-standard processing." Its "standard" processes are licensed by GTE, Plessey, and Eurasil, among others. Mitel is changing to 4" (diameter) wafer-production capability.
No minimum.	Masks to packaged devices (typical): 6 to 7 weeks for bipolar devices, 5 to 6 weeks for metal-gate MOS, 8 to 10 weeks for silicon-gate CMOS. "Expedited turnaround" can also be arranged.	Supplied by foundry.	Outside designers should interface with Monosil *before* starting the design. The company provides design rules and process/design criteria.

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Mosfet Micro Labs, Inc. Penn Center Plaza Quakertown, PA 18951 (215) 536-2104 Robert Campbell Marketing Manager	MM	x 5μm (also tungsten gate process)	x 5μm	x 5μm	x 5μm	x 5μm (also tungsten gate process)	x 5μm	x I²L	Masks.
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 737-6055 Richard T. Barck Director of Marketing, Custom MOS	NS	x 5μm	x 4 to 5μm 3μm	x 8μm		x 7μm	x 4μm single and dual poly	x Junction-isolated processes: I²L, 5V Schottky, 5-100V non-Schottky, 5V gold-doped. Oxide-isolated processes: I²L and 5V Schottky.	Database tapes, masks, PG tapes.
Nitron 10420 Bubb Road Cupertino, CA 95014 (408) 225-7550 Robert D. Miller Vice President Marketing	NI			x 7μm		x 7μm	x 4 to 5μm		Reticles, PG tape.
Plessey Semiconductors 1641 Kaiser Avenue Irvine, CA 92714 (714) 540-9979 John M. Stratford Product Marketing Manager	PL		x 4μm				x 4μm Iso-CMOS	x I²L, ECL 2μm	CIF file, PG tape (Mann 3000 series), masks.
Polycore Electronics, Inc. 1107 Tourmaline Drive Newbury Park, CA 91320 (805) 498-8832 S.K. Leong Vice President	PE					x 8V, 20V threshold processes		x Linear, I²L, TTL	Database tape (Calma) or masks.
Precision Monolithics, Inc. 1500 Space Park Drive Santa Clara, CA 95050 (408) 727-9222 Richard Corbin, Director Custom Wafer Fabrication	PM						x 4μm	x Linear (20V to 60V), I²L (6V to 12V), ECL (washed-emitter)	PG tape, database tape, masks (prefers working plates or sub-masters).
RCA Route 202 Somerville, NJ 08876 (201) 685-6798 Jim Hively, Director of Semicustom Operations	RC					x 7μm	x 3μm (Also 3μm CMOS-SOS)	x I²L, standard bipolar	Calma or Applicon database tape.
Semi Processes Inc. 1885 Norman Avenue Santa Clara, CA 95050 (408) 988-4004 Charles B. Detrick Wafer Service Manager	SP					x 6μm	x 5μm (currently bringing on-line)		Masks, PG tape (prefer masks).
Senitron Corporation 3883 North 28th Avenue Phoenix, AZ 85017 (602) 277-3481 Brent R. Fox President	SC	x 5μm	x 5μm	x 5μm	x 5μm	x 5μm			Sub-master masks, PG tape, database tapes (prefer sub-master masks).
Signetics Corporation 811 E. Arques Avenue P.O. Box 409 Sunnyvale, CA 94086 (408) 746-1855 Joe Stern Product Marketing Manager	SG							x STL,ISL,ECL Junction and oxide-isolated (3μm minimum features)	Database tape (*e.g.*, Calma), PG tape, masks.

Minimum Production Run	Turnaround Time	Process Control Monitor	Special Capabilities or Considerations
Maximum: 100 wafers (3")/month	Information not available.	Supplied by customer.	MML processes wafers from masks. Period. The company does no mounting or bonding. MML is a prototype fabrication house; all fabrication processing performed by engineers and technicians.
Minimum business per design *family*: $150,000 to $200,000/year. Not interested in prototype business *only*; production-volume business instead.	Database tape to PCM-tested wafers: 6 to 10 weeks (depends on on process.)	Supplied by foundry (the design rule specifications includes PCM information).	National guarantees to hold existing processes for five years. In-house developed ERC (electrical-rules check) program is available to foundry customers. Like Intel, National is clearly looking for high-volume business.
Production run (other than qualification run): 5000 devices (minimum). Qualification run: 25 wafer starts (typical).	Reticles to packaged, untested prototypes: 8 weeks. Reticles to tested production parts, assuming prototypes are acceptable: 16 to 18 weeks (typical).	Supplied by foundry or by customer (preferably by foundry).	Nitron has many years of experience in fabricating mil-spec ICs from U.S. government-supplied tooling. The CMOS Si-gate line is presently an "R&D" module" with capacity of 1000 4" diameter wafers/week. In 2 to 3 years, expect to have greater Si-gate CMOS production capacity.
Minimum individual run: 5 to 100 wafers. Annual commitment required: 100 to 5,000 wafers. (Depends on whether the process is standard or non-standard).	Database tape in to packaged chip out: 6 to 14 weeks (typical).	Supplied by foundry.	A process engineer is assigned to each group of designs from a given customer. Plessey plans to have 3μ MOS fabrication capability by the end of 1982. The company provides outside designers with design rules, and encourages interaction with Plessey staff during the design phase.
No minimum.	From masks to wafers: CMOS: two working weeks. Bipolar: 3 to 4 working weeks.	Supplied by foundry or by customer.	Polycore manufactures ICs for pacemakers. Equipment and process documentation conform to MIL 38510 standards. The company can assemble and test sample chips. Provides weekly updates to customers regarding process status of jobs.
Engineering lot: 5 wafers out. Minimum production run: 100 wafers. (PMI does not want to run engineering lots without assurance of a production order.)	Turnaround time, working plates to delivered wafers: 4 to 6 weeks, depending on the technology.	Supplied by foundry or by customer.(PMI has PCM for CMOS and linear technology, but not for I^2L or ECL.)	PMI has a 2-layer metal process available for bipolar designs, and thin-film (Si-chrome) resistors for every technology except washed-emitter ECL. Design rules for all processes are available upon execution of a non-disclosure agreement.
Minimum prototype run: 50 wafers. Production runs: 1000 wafers.	Best case, database tape to wafers: 10 weeks. (Depends on quality of input.)	Supplied by foundry.	Interface should begin with "face-to-face" meeting at which RCA's engineers are involved in a design review. One of the few companies offering CMOS-SOS.
Prototype run: 20 3" diameter wafers (typical).	Prototype runs (masks to wafers): CMOS ,metal-gate: 4 to 6 weeks (typical). CMOS silicon-gate: 8 to 10 weeks (typical).	Supplied by customer.	Published rules are available for the older metal-gate process (the silicon-gate process is considered proprietary). An engineer is assigned to follow each C.O.T. order. Typically, 2 runs—one week apart—are processed for the engineering run. SPI plans to have a 5" wafer processing line operating by mid-1983.
Minimum production run size: 50 to 100 wafers/month (per device type, average). (Does not want to process prototype runs *only*.)	Sub-master masks to packaged, untested prototypes: 4 weeks (typical). Add 2 to 4 weeks for production parts.	Supplied by customer. (Senitron is also developing its own proprietary PCM.)	Senitron purchased GTE Microcircuits' older 3" wafer fabrication facility in May 1981. Unlike the larger semiconductor makers, Senitron plans to make its niche in "mature" MOS technologies, acting as a foundry for processes that are being discontinued by the larger semiconductor manufacturers, and as a foundry for ROMs.
Prototype: 12 4" diameter wafers (minimum). (Would not do a prototype run without a production commitment.) Production run: 50/delivery (minimum, for total of 250 wafers/year.)	Masks to shippable (PCM tested)wafers: 8 weeks. (Add 4 weeks if input is Calma data base tape.)	Supplied by foundry or by customer (preferably by foundry).	Signetics will make a simplified set of design rules available, in data-sheet format. It will also give customers details (database tape, test data) of its PCM. In the near future, Signetics may also offer MOS foundry services, although plans have not been formally announced.

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Silicon Systems, Inc. 14351 Myford Road Tustin, CA 92680 (714) 731-7110	SI					x 5V, 15V (analog/digital)			Calma database tape, PG tapes, masks
Solid State Scientific, Inc. Montgomeryville Industrial Ctr. Montgomeryville, PA 18936 (215) 855-8400 Allen W. Hyman Marketing Manager Custom Products	SS		x 7μm			x 8μm	x 6μm		Database tape, PG tape, reticles, or masks.
Solitron Devices, Inc. 8808 Balboa San Diego, CA 92123 (714) 278-8780 Customer Service	SD			x 5μm		x 5μm		x Linear 5μm	PG tape, database tape, masks.
Standard Microsystems Corp. 35 Marcus Boulevard Hauppauge, NY 11787 (516) 273-3100 Less Penner Marketing Manager Custom Circuits	SM		x 4μm	x 6μm					Calma database tape, PG tape, masks. (Prefers Calma database tape so can "edit around the fringe," *i.e.*, add critical dimension layout, alignment marks, etc.)
Storage Technology Corp. 2320C Walsh Avenue Santa Clara, CA 95051 (408) 727-3503 James A. Horton Applications Manager	ST						x 3μm	x Linear	Masks.
Supertex, Inc. 1225 Bordeaux Drive Sunnyvale, CA 94086 (408) 744-0100 Richard Siegel Vice President/Sales	SX			x 5μm		x 5μm	x 5μm		Masks.
Synertek (A subsidiary of Honeywell, Inc.) 3001 Stender Way Santa Clara, CA 95051 (408) 988-5600 Denise Gavin Welsh COT™ Marketing Manager	SY		x 6μm 5μm 4μm				x 3μm		Database tape, PG tape, masks.
Universal Semiconductor, Inc. 1925 Zanker Road San Jose, CA 95112 (408) 279-2830 Barry Boulton	US						x 5μm Iso-CMOS, 3μm Hiso-(double poly)		Database tape, PG tape, masks.
VLSI Technology, Inc. 1101 McKay Drive San Jose, CA 95131 (408) 942-1810 George Steres COT Program Manager	VT		x 4μm, 3μm HMOS-I				x (4μm Iso-CMOS)		For MPW (multi-product wafer: CIF For production: CIF, database tape (Calma, Applicon), PG tape, masks.
ZyMOS P.O. Box 62379 Sunnyvale, CA 94088 (408) 730-8800 William Loesch Director of Marketing	ZM		x 5μm			x 6μm	x 5μm		Database tape, masks.

Minimum Production Run	Turnaround Time	Process Control Monitor	Special Capabilities or Considerations
Min. engineering order: 12 wafers out. Min. production order: 75 wafers out.	PG tape to wafers: 8 weeks (standard), 6 weeks (expedited). Add 1 week for prototype devices. Add 4 to 7 weeks for production devices.	Supplied by foundry.	Computerized management information system tracks work in process. SSI plans to have a bipolar 2-layer metal Schottky process running by late 1982, and bipolar 2-layer metal "washed emitter" Schottky and 5V CMOS silicon-gate processes by early 1983.
Production volume minimum: 15,000 to 25,000 devices/year.	Masks to working, tested parts: 8 to 10 weeks (typical). PG tape (Mann) to working, tested parts: 11 to 13 weeks (typical).	Supplied by foundry.	Recommends working with SSSI before starting chip layout. Establishes "direct lines of communication between our engineering staff and the customer."
Minimum run: 1 lot (25 wafers).	Turnaround time, working plates to PCM-tested wafers: 6 to 7 weeks (typical).	Supplied by customer.	Does Mil Standard 883 processing. Will also modify processing (threshold voltages, thin oxides, deep diffusions, etc.) to customer requirements. Conservative set of design rules generally available without requirement of non-disclosure agreement.
Minimum run: 25 wafer starts, 18 wafers out guaranteed. (Minimum requirement is larger if design rules are non-standard.)	Masks to wafers: 4 weeks (typical). Calma tape to wafers: 8 weeks (typical). (Packaging adds about 1 week.)	Supplied by foundry. (Customer's PCM may be used in limited cases for the first run.)	"We'll provide the design rules at the drop of a hat if if the customer signs a non-disclosure agreement." Company scribes a number on the back of each individual wafer and maps the wafers individually. Computerized PCM analysis.
Prototype run: 20 wafers (4")	Masks to PCM-tested wafers: 6 weeks (typical).	Supplied either by foundry or by customer (preferably by foundry).	STC began offering foundry services in February 1982, as an offshoot of its gate array manufacturing line. One of the few foundries offering 2-layer metal.
Minimum production run: 1 lot (up to 24 wafers) (non-Supertex-standard processes require a price quotation from factory).	Masks to PCM-tested wafers: 4 to 6 weeks (typical). (2½ to 3 weeks at 50 % additional cost.)	Supplied by foundry or by customer.	Also offers DMOS and combined CMOS/DMOS silicon- gate processes.
Prefers to ship fully tested and packaged parts in quantities of 25,000/ year, but will "look at other deals and make a business decision."	Database tape to "cut and go's": 10 weeks. PG tape to "cut and go's": 8 weeks. Masks to "cut and go's": 3 to 5 weeks.	Supplied by foundry.	Synertek calls this the C.O.T™ business. A 3-micron HMOS (nMOS) line should be available in the fall of 1982. A double-poly CMOS process is scheduled for the first half of 1983. E^2PROM technology (5 micron, 3 to 9V) is also being developed.
Minimum prototype run: 50 wafers.	Masks to probed wafers: 6 weeks. Masks to production parts (packaged, tested): 9 weeks.	Supplied by foundry or by customer (preferably by foundry).	Although Universal developed its processes independently, a company spokesman says that it has customers in common with AMI. Universal recently decided to drop its nMOS line and concentrate entirely on silicon-gate CMOS.
Minimum MPW run size: 25 packaged, untested units. Prototype run (stand-alone product): 5 wafers out minimum. Production lot size (min.): 24 wafer starts.	MPW: From database merge to packaged prototype (no test): 5 to 8 weeks. Single product: 2 weeks from masks to wafers.	Supplied by foundry.	VTI's processing facility is now scheduled to come on-line in early September 1982, several months behind the original schedule. The company will offer low-cost "MPW" capability, in addition to more traditional services. It will also offer access to design tools. The company will process a proven "canary" product (*e.g.*, a 64K ROM) on the MPW to verify yield and performance.
Minimum prototype run: guarantee 6 4" diameter wafers out.	Masks to wafers (PCM tested only): 3 to 4 weeks. Database tape to wafers (PCM tested only): 6 to 8 weeks. Masks and Sentry VII test tape to packaged, tested chips: 8 to 10 weeks.	Supplied by foundry or by customer.	One of the newest fabrication facilities around, ZyMOS, (along with AMI) has processed several multi-project wafers.