Silicon Foundry Status Report

Just over a year ago (Jansen and Fairbairn, 1981), *VLSI DESIGN* (then *LAMBDA*) defined the "silicon foundry," and described the progress toward a "hypothetical" foundry—one in which a clean interface exists between a chip designer and a silicon fabricator. One premise of that article was that because mask and fab considerations were (and, presumably, still are) irrelevant to the chip-design process, the foundry should effectively "hide" such details from the designer.

That scenario is certainly an appropriate *goal*; but we have not quite reached it. However, the following circumstances indicate that the commercial world is beginning to recognize the need for a clean separation of *design processes* from *implementation*:

- Large semiconductor companies are talking more and more about their "silicon foundry" or "customer-owned tooling" services.
- Some companies are starting to offer outside designers "simplified" design-rule sets, instead of design books that are each the size of the Gutenberg Bible.
- The activity of silicon "brokers"—such as USC's Information Sciences Institute (ISI) (see "Quality Control From the Silicon Broker's Perspective" in this issue) and SynMos (Mountain View, CA)—is picking up. Such brokers often handle the mask/fab details that can "bite" chip designers (especially novice designers).
- One consultant (R.C. Anderson) recently put together a "standardized" IC design and procurement system (see *Literature Review* in this issue), that could make it easier for chip designers to interface with a stable of foundries.

Foundries for the "Little Guy"

The *Survey of Silicon Foundries* that appears on pages 42 through 49, includes some large semiconductor companies (*e.g.*, Intel, Signetics, and Intersil), but not others (*e.g.*, Motorola, Fairchild, and TI). This should not be taken as a black-and-white distinction between the two groups—whether specific large companies are (or should be) included in our survey is as much a matter of semantics as of downright fact.

For example, in response to *VLSI DESIGN*'s query, a TI spokesman said: "If we do get involved [in the foundry business], it's usually with a major program which can fit into our standard process flow." Interestingly, although TI cannot be considered a commercial silicon foundry (since it only *selectively* offers high-volume foundry services) it does act as a prototype (low-volume) foundry for at least one university: Texas A&M (see *University Scene* in this issue).

Other large companies *are* included in our survey because they are actively soliciting this type of business. But be careful! Unless these firms see a "carrot" in the form of a lot of business down the road, they may not be interested in prototyping (or other small-volume) business. Luckily, though, as our survey shows, many firms *are* willing to supply chips in low-to-medium volume.

For very low volume jobs (say, twenty or fewer parts), the number of available foundries falls sharply. One alternative is to go to a commercial "silicon broker." SynMos, one of the first of these brokers, will return 10 silicon-gate, 5-micron-design-rule, nMOS packaged devices (with verified fabrication, but without functional testing of the devices) for $3,000. (Die size: 150 mil^2—other die sizes are priced accordingly.)

Remaining Difficulties

Although efforts clearly are being made to improve the interface between designers and foundries, many problems still remain. For example, some foundries offer state-of-the-art processing to outside designers, but will not release design rules for any but their most mature processes.

As our survey shows, nothing exists that even remotely approaches a standard data-interchange format. Some companies prefer high-level descriptions (CIF, Calma format); others want tooling (masks) only. Nor is there any consensus about whether the designer (customer) or manufacturer (foundry) should provide the process-control monitor (PCM). In some cases, *two* PCMs end up on wafers—further reducing the amount of wafer area available for "useful" dies. Unfortunately, instead of using a "universal" PCM, most chip fabricators have a "pet" PCM that is tweaked for their specific process or fab line.

Then, too, not all silicon foundries have the same "back-end" services. Some have complete wafer and packaged device testing facilities, while others consider that their job is done once the wafers meet the PCM criteria.

Perhaps the *main* problem that designers will have in interfacing with foundries is that the jargon and subtleties of the silicon-process line (and the problems that can creep up) are often foreign (to the designers). In the reports that follow, *VLSI DESIGN* will acquaint designers with precisely these considerations. Steve McMinn (page 16) offers the silicon foundry's perspective, and suggest several techniques that designers may want to keep in mind to increase the likelihood of a successful silicon implementation on the first pass. Danny Cohen and Vance Tyree (page 24) explain (from the silicon broker's perspective) ways to monitor the quality of an implementation run from design-input-in through packaged-chip-out.

—Jerry Werner

References:

Jansen, W.D., and D.G. Fairbairn. First Quarter 1981. "The Silicon Foundry: Concepts and Reality," *LAMBDA* (now *VLSI DESIGN*).