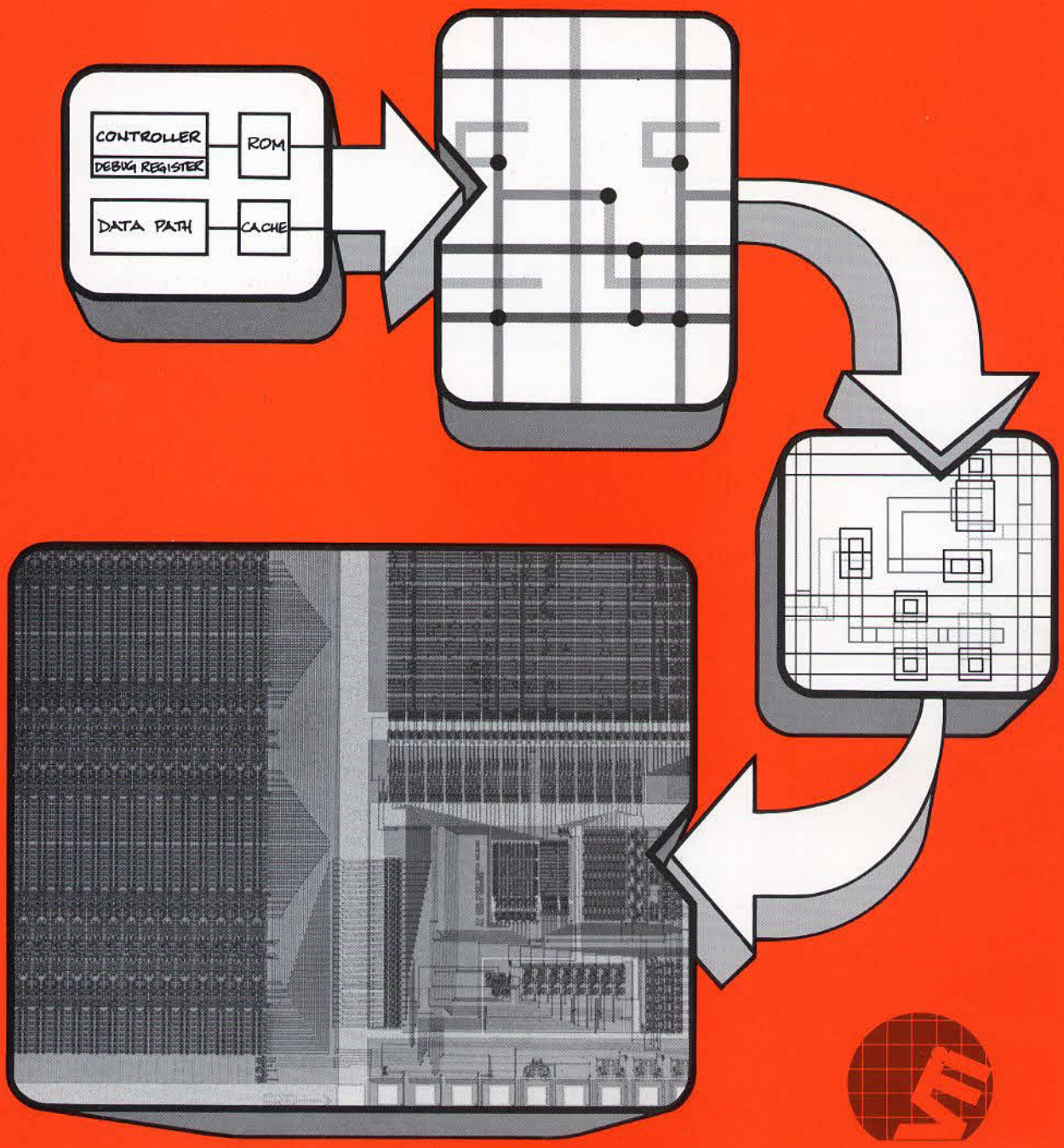
VLSI Technology, Inc. invites you to participate in an intensive course on

User-Designed™ VLSI Systems.

September 28, 1981 — October 23, 1981

Santa Clara, California



VLSI Technology, Inc.
3101 Scott Blvd.
Santa Clara, CA 95051
(408) 727-3108

User-Designed™ VLSI

Design Control...

User-designed VLSI means **you** do the design. You maintain design control and optimize the architecture and performance in ways only an expert in your field can. You **minimize** product **development time** by designing the system once. No need to design it in TTL first and then have someone else (who doesn't understand it) redesign it for VLSI.

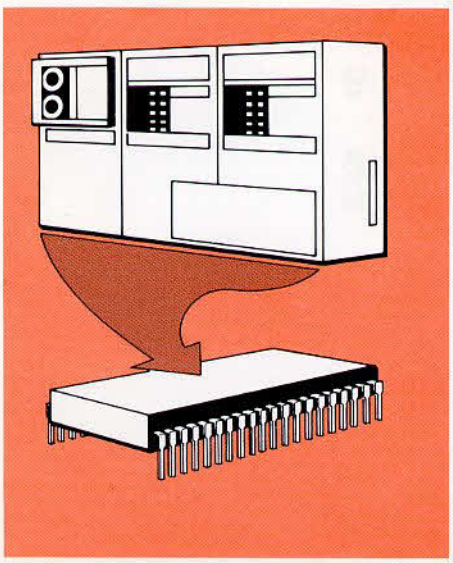
High Productivity...

Through the use of a **new design methodology**, pioneered by Prof. Carver Mead of Caltech and Lynn Conway of Xerox, digital systems designers and programmers can take advantage of the high density, high performance, and low cost of VLSI custom circuits, while achieving shorter design cycles and greater productivity than is possible with other custom design approaches. This new methodology, with its improved productivity, means that **low volume custom VLSI** is now practical!

VLSI Architectures...

The Mead-Conway approach emphasizes the importance of choosing system architectures appropriate to VLSI, and the effect of architecture on system performance. This philosophy is formalized in a design methodology that deals with the critical issues of chip-complexity management, and the top-down design of modules and inter-module communications.

This is the design methodology of the '80s and will support your company's product needs for the rest of the decade.



Benefits

Benefits of User-Designed VLSI...

User-designed VLSI offers significant advantages over the various design alternatives available to the electronic system designer in the 1980's. This technology benefits you, your products, and your company.

Benefits to Your Company...

VLSI-based products offer many advantages to your company. They are generally more competitive and provide higher margins than products based on older technologies. User-designed VLSI means lower design costs and earlier market entry for your VLSI-based products.

Benefits to Your Products...

VLSI can vastly reduce product size and cost while offering increased performance and unique features that your competition won't be able to duplicate easily. User-designed VLSI means you can capitalize on these benefits while at the same time protecting your proprietary system knowledge, keeping design times and costs under control, and maintaining independence of outside design firms. Compared with other technology alternatives such as gate arrays, user-designed VLSI offers an approximate 10 to 1 density advantage.

Benefits to You...

In a technology that is moving as fast as VLSI, it is tremendously difficult to keep current with the latest advances. This course will provide you a design-level understanding of VLSI and VLSI CAD tools. This course is not an overview; it is not a survey of what others are doing. It is intended to provide you with a unique set of knowledge and skills that will make you a much more valuable contributor to your company's strategic plans and products. The course requires only a modest digital design or programming background, and allows you and your company to become participants in the LSI/VLSI design revolution.

Take a leadership role — design your systems in silicon!

VLSI Technology, Inc.

A New Kind of Semiconductor Company

VLSI Technology was founded to pursue semiconductor markets that will see substantial growth as the industry approaches Very Large Scale Integration (VLSI). Specifically, the company will concentrate on products and services for two segments of the MOS market: custom and customizable (or programmable) devices. To competitively participate in these market segments, a supplier must first have a high-technology base (both people and products), and second provide quick-turnaround services. A different kind of MOS company is needed, and VLSI Technology intends to be the first to properly service this market.

User-Designed VLSI Services...

VLSI Technology will soon be offering a complete set of capabilities for the user-designed VLSI community: **training, design tools,** and **silicon foundry services.** Our course offerings will expand to include quarterly courses in both nMOS and CMOS design in 1982. Instructional material and design tools to support courses at your own facility will also be available. Those of you interested in setting up a VLSI training activity in your facility will find this course an extremely good way to get that activity started. Participants in this course will make excellent instructors or tutors for later in-house courses. A remote-entry silicon foundry service will be operational in 1982 to meet both your prototyping and production needs.

Other Products and Services...

In addition to user-designed VLSI services such as this course, VLSI Technology will soon offer a full line of semiconductor services, including an electronic front-end silicon foundry, electron-beam mask making, advanced **nMOS** and **CMOS** processes for custom circuits, a **custom IC design** capability, fast-turnaround processing, and a full-complement of high-density **mask-programmable ROMs.**

VLSI Technology is a new kind of MOS IC company preparing to support the user-driven demand of the 1980's.

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Course Description

A Unique Course...

This intensive, one-month, multi-media course in user-designed VLSI systems teaches you to architect, design, and layout your own proprietary systems on silicon. Specific topics covered include basic nMOS logic design, two-phase clocking systems, PLA's and finite state machines, digital subsystems and chip floor plans, chip planning and layout, timing and power dissipation calculations, memory subsystems, nMOS processing and design rules, and new developments in design automation for VLSI. For the first time, this course is backed by the experience of a semiconductor company fully committed to the user-designed VLSI marketplace.

Who is the Course For?

The course is aimed at digital systems architects, designers, and system programmers interested in discovering what VLSI can do for them and the systems they design. No previous experience in IC design is required, however, a modest programming background is extremely valuable. Systems programmers with no previous hardware design experience often find this course extremely interesting and rewarding.

An Intensive Course...

This four-week course will require your full attention. The first week will be devoted to lectures and homework assignments. The following three weeks will be devoted almost entirely to work on an actual IC design project. Following the conclusion of the course, the **completed chips** that result from the class **will be** fabricated by VLSI Technology, and **returned to the students** for testing. All fabrication and packaging for these course-generated designs is included in the course fees.

Quality Instruction...

In addition to live instruction by Douglas Fairbairn and other VTI personnel involved in CAD tool development and chip design, a number of well-known experts in the VLSI design field appear during the video tape segments of the course. These instructors include Prof. Carver Mead of Caltech, Lynn Conway of Xerox, Profs. Robert Mathews, John Newkirk, and James Clark of Stanford, Prof. Charles Seitz of Caltech, and Jack Holloway of Symbolics, Inc.

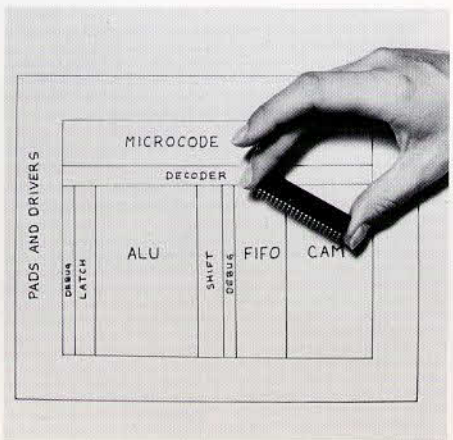
The instructors for the course have debugged the material over the past two years while teaching VLSI design courses at M.I.T., Caltech, Stanford, U.C. Berkeley, Xerox, Hewlett-Packard, and Evans and Sutherland Computer Corporation. Similar courses in the Mead-Conway VLSI design methodology have been, or are now being taught, at such industrial sites as Digital Equipment Corp., Varian, Bell Labs, and many others. In addition, courses based on this methodology are now being offered at over 60 major universities in the U.S. and Europe.

A Rich Environment...

An exciting aspect of the course will be that it is the first one of its kind to be offered by a semiconductor company at its own facility. You will have contact with a wide variety of people active in both VLSI design and VLSI design tool development. This rich environment will contribute greatly to the learning process.

Your Design in Silicon!

The design phase of the course is an essential part of the overall learning experience. It is only during this phase that you understand how the tradeoffs of architecture, circuit design, and layout interact and where the real challenges and opportunities of VLSI lie. It's the kind of understanding you will never get by reading trade journals and attending seminars. The final step that lends excitement and credibility to the design phase is that the circuits are merged together on an E-beam mask set and fabricated using a high-technology nMOS process. The individual student projects are then packaged in standard dual-in-line packages and returned to you for testing after the conclusion of the course. **Don't miss the opportunity to have your ideas cast into silicon!**



Return Home with Your Design in Silicon.

Supporting Material...

The course text is **Introduction to VLSI Systems** by Mead and Conway (Addison-Wesley, 1980). In addition to the text, we have a complete set of lecture notes that complement the video tapes used for some of the lectures. Other reading material from the current literature will be furnished as appropriate.

Course Schedule and Format...

This course will be held in a specially equipped lab and classroom at VLSI Technology in Santa Clara, California. Unlike other courses you may be familiar with, this one will require your full-time attention for four weeks. The first week of class will involve lectures, discussions, and homework assignments. The following three weeks is the project phase of the course and will be devoted to work on an IC design project of your own choosing. Typical projects completed by students consist of a few hundred to a few thousand transistors. These circuits might be a serial multiplier, a special-purpose graphics function, a content-addressable memory, or a project of similar complexity.

Normal class hours will be 9 a.m. to 5 p.m., 5 days a week. The CAD laboratory facilities will be available from 7 a.m. until 11 p.m., 6 days a week.

The Instructor

The principal instructor for the course is Douglas Fairbairn. Mr. Fairbairn has been active in the user-designed VLSI field since 1976 and helped develop the design methodology used in this course while working at the Xerox Palo Alto Research Center. He has designed LSI chips from architecture to final layout, co-authored a CAD program for VLSI layout, and taught VLSI design at Xerox, Caltech, Hewlett-Packard, and Evans & Sutherland Computer Corporation. He also has significant experience as a systems engineer, including a variety of distributed processing experience.

Mr. Fairbairn helped found VLSI Technology in 1980, and now serves as Manager of VLSI Engineering. He is responsible for all VLSI course and design-tool development as well as all silicon-foundry related software.

Course Outline

A Perspective on VLSI Design

Before diving into the detailed design material, it is important to gain an overall perspective of how VLSI design is different from designing chips of lesser complexity. One of the major points of difference is just that — complexity. We will focus on the importance of hierarchical design and regular structures as an answer to this fundamental problem.

Introduction to nMOS Logic Design...

We open the technical discussion with two lectures on the basic design techniques used in nMOS logic design. We cover switch logic, gate logic, stick diagrams, device ratios, and basic design strategies.

Registers and Two-Phase Clocking Systems...

A straight-forward and reliable clocking system is introduced for driving synchronous digital systems. Example applications include a hardware first-in, first-out stack.

PLAs and Finite State Machines...

PLAs provide a way of mechanizing sets of arbitrary Boolean equations in a geometrical and conceptually regular way. Moreover, with the addition of clocking, they become finite state machines. Detailed examples are given.

Digital Subsystems and Chip Floor Plans...

The basic logic building blocks of nMOS design including ALUs, shifters, register cells, function blocks, etc, are described.

Chip Planning and Layout...

The importance of an overall chip plan is emphasized, with particular attention focused on the communications paths of the chip. Detailed examples are provided.

nMOS Scaling and its Implications for Design...

Much has been discussed in recent years concerning the physical limits to scaling. Here we'll take a look at the scaling process and see what effects it will likely have on design.

Timing, Delays, and Power Dissipation...

Calculation of propagation delays through logic structures and resistive interconnects are covered. Techniques for minimizing these delays at both the system and circuit level are explored. The role of detailed circuit simulation in the design process is also described. Calculation and minimization of power dissipation is covered along with power busing considerations.

Memory Subsystems...

A wide variety of memory subsystems are explored, including shift registers, static RAM cells, and dynamic RAM cells. These approaches are compared in terms of size, speed, power dissipation, and ease of design. Design examples are provided.

System Design Examples...

Examples from a variety of disciplines including signal processing, general-purpose computation, and graphics processing are presented.

nMOS Processing and Design Rules...

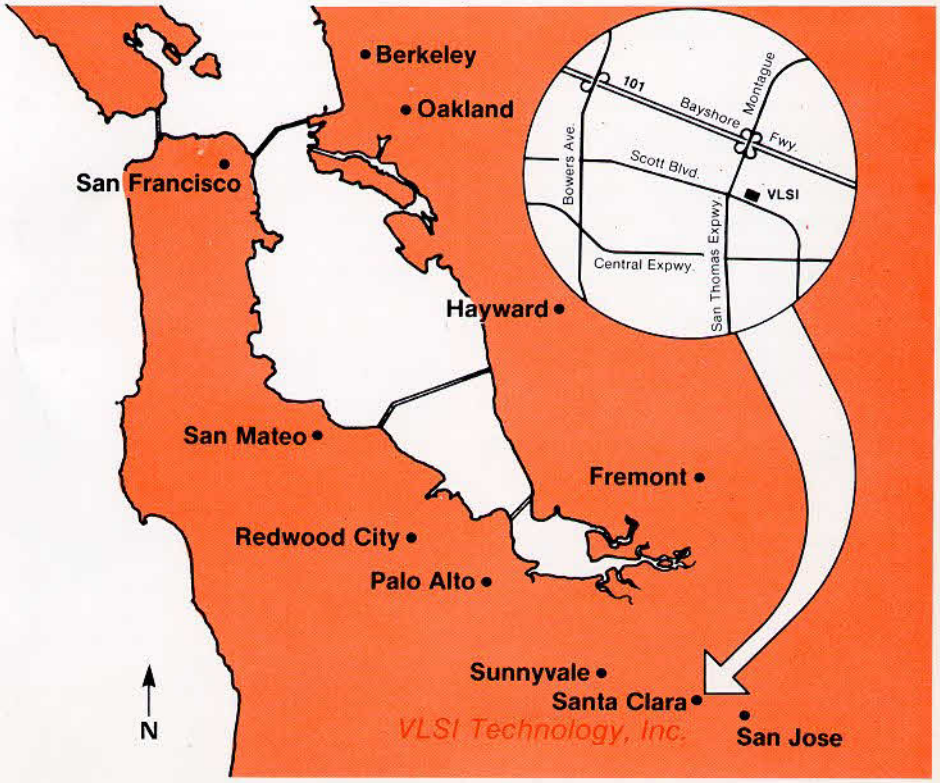
We introduce the basic process steps of nMOS fabrication and relate those to the development of the geometrical design rules that guide the layout of integrated circuits.

Design Automation...

Progress in design automation tools is critical to the widespread adoption of user-designed VLSI. During the course we will look at the design automation alternatives in detail and study some of the new developments such as silicon assemblers and compilers, Sticks symbolic layout systems, procedural design techniques, etc. Students will use some of these tools in the design and analysis of their own project chip during the course.

The Silicon Foundry...

We will examine the silicon foundry concept and describe its role in the industry. Multi-project chip wafers, the Caltech Intermediate Form (CIF), standard test devices, and silicon implementation services will be among the topics described.



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