MPC79 Chip Photos

A VLSI Archive Page compiled by Lynn Conway [V 11-20-07].

Historical background:

Following the success of her M.I.T '78 VLSI design course, Lynn Conway sought ways to dramatically scale up internet access to quick-turnaround chip prototyping, in order to enable wider testing, refinement and evaluation of the new Mead-Conway design methods. In the spring of 1979 she conceived of a new type of internet-based implementation infrastructure for this purpose, and announced its availability to students taking Mead-Conway courses in the fall of ’79.

In a crash-effort that summer at PARC, Alan Bell and Martin Newell created a software prototype of the new "MPC System". Lynn's team used the new system to support rapid prototyping of student design projects at many universities that fall, in a large-scale experimental demonstration-trial of the new VLSI design and implementation methods called "MPC79". MPC79 played a vital role in the rapid evolution and validation of the Mead-Conway design methods, and the rapid propagation of the methods into over 100 universities and scores of startup companies within just several years.

This file contains scans of the original MPC79 chip photos, along with pages from the MPC79 Implementation Documentation that locate and identify project die-types and individual projects. High resolution JPGs of each die-type can be accessed via the links below and via the VLSI Archive Spreadsheet.

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Links to high-resolution JPGs:
AB, AC, AD, AE, AF, AG, BI, BJ, BK, BL, BM, BN, BK-8, BK-5
MPC79 Multiproject Chip Layouts
List of wafer-die-project codes and corresponding project ID's

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<td>AB-7 PicardMIT</td>
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<td>AB-8 AllenMIT</td>
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<td>AC-1 HamiltonMIT</td>
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<td>AC-2 PaesmanMIT</td>
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<td>AE-2 ClassUI</td>
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<td>AE-3 MurrayOT</td>
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<td>AE-4 RogersOT</td>
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<td>AE-5 FehlingCMU</td>
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<td>AE-6 KungCMU</td>
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<td>AE-9 KehlOT</td>
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<td>AP-1 Schip2</td>
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<td>AG-1 WalpCT</td>
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<td>AG-2 KathailMIT</td>
<td>BK-7 BechtoldsheimSU</td>
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<td>AG-3 RiversMIT</td>
<td>BK-8 ClarkSU</td>
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<tr>
<td>AG-4 SnyderOT</td>
<td>BL-1 HellerCT</td>
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<td>AG-5 GoddeauMIT</td>
<td>BL-2 EatonCT</td>
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<td>AH-1 LHDoc1</td>
<td>BL-3 WatteyneCT</td>
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<tr>
<td>AH-2 RHDoc1</td>
<td>BL-4 MostellerCT</td>
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<td>BL-5 GrayCT</td>
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<td>BL-6 PinesCT</td>
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<td>BL-7 DerbyCT</td>
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<td>BL-8 PedersenCT</td>
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<td></td>
<td>BM-1 LigockiCT</td>
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<td></td>
<td>BM-2 DeuuirUCB</td>
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<tr>
<td></td>
<td>BM-3 FungUCB</td>
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<tr>
<td></td>
<td>BM-4 LandmanUCB</td>
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<tr>
<td></td>
<td>BM-5 RumphUCB</td>
</tr>
<tr>
<td></td>
<td>BM-6 EllisCT</td>
</tr>
<tr>
<td></td>
<td>BM-7 SequinUCB</td>
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<tr>
<td></td>
<td>BN-1 WatanabeUR</td>
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<tr>
<td></td>
<td>BN-2 LyonsUR</td>
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<td></td>
<td>BN-3 KedemUR</td>
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<tr>
<td></td>
<td>BN-4 SohnUR</td>
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<tr>
<td></td>
<td>BN-5 TüneUEUR</td>
</tr>
<tr>
<td></td>
<td>BN-6 UtsSU</td>
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<tr>
<td></td>
<td>BN-7 TarsSU</td>
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<tr>
<td></td>
<td>BO-1 LHDoc1</td>
</tr>
<tr>
<td></td>
<td>BO-2 RHDoc1</td>
</tr>
</tbody>
</table>
## List of Designers and their Projects

**CALTECH:**

[Summary of designs from CalTech, updated 4-Dec-79 23:13:17]

<table>
<thead>
<tr>
<th>Designer</th>
<th>Description</th>
<th>Reserved space</th>
<th>Area</th>
</tr>
</thead>
</table>
| BJ-5 BartonCT | Designer: Eric Barton  
Description: LED array driver  
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm | |         |
| BJ-8 BozzutoCT | Designer: Rick Bozzuto  
Description: Pulse width to binary converter  
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm | |         |
| BJ-1 CampbellCT | Designer: James Campbell  
Description: Logical processing unit with internal registers  
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm | |         |
| BJ-6 CocconiCT | Designer: Alan Cocconi  
Description: Array processor  
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm | |         |
| BL-7 DerbyCT | Designer: Howard Derby  
Description: Associative Memory  
Reserved space = 2170 x 2566 microns, Area = 5.57 sq mm | |         |
| BL-2 EatonCT | Designer: Steve Eaton  
Description: Counter/adder  
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm | |         |
| BM-6 EllisCT | Designer: Mike Ellis  
Description: Stepping motor controller  
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm | |         |
| BJ-2 FuCT | Designer: Sai Wai Fu  
Description: Square root generator  
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm | |         |
| BL-5 GrayCT | Designer: Moshe Gray  
Description: Array processor  
Reserved space = 2534 x 2082 microns, Area = 5.28 sq mm | |         |
| BL-1 HellerCT | Designer: Jack Heller  
Description: Digital filter  
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm | |         |
| BJ-10 HoCT | Designer: Kuo Ting Ho  
Description: 10 bit rate multiplier  
Reserved space = 2120 x 1110 microns, Area = 2.35 sq mm | |         |
| BJ-9 KingsleyCT | Designer: Chris Kingsley  
Description: Serial Multiplier  
Reserved space = 2200 x 2064 microns, Area = 4.54 sq mm | |         |
<table>
<thead>
<tr>
<th>Device</th>
<th>Designer(s)</th>
<th>Description</th>
<th>Reserved space</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJ-4 LiCT</td>
<td>Peggy Pey-Yun Li</td>
<td>Two's-complement pipeline multiplier</td>
<td>2176 x 1326 microns, Area = 2.89 sq mm</td>
<td></td>
</tr>
<tr>
<td>BM-1 LigockiCT</td>
<td>Terry Ligocki</td>
<td>Scan converter chip</td>
<td>2000 x 4108 microns, Area = 8.22 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-4 MostellerCT</td>
<td>Rick Mosteller, Greg Eflan, Dick Lang</td>
<td>Stack-oriented microprocessor</td>
<td>4300 x 2996 microns, Area = 12.88 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-3 PapachCT</td>
<td>A.C. Papachristidis</td>
<td>Magnitude comparator</td>
<td>2000 x 1126 microns, Area = 2.25 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-8 PedersenCT</td>
<td>Bruce Pedersen</td>
<td>Asynchronous FIFO</td>
<td>1896 x 2000 microns, Area = 3.79 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-6 PinesCT</td>
<td>Elliot Pines</td>
<td>Expandable clocking pattern generator chip</td>
<td>1780 x 1780 microns, Area = 3.17 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-7 PursifullCT</td>
<td>Ralph Pursiful</td>
<td>Self-Timed Queue</td>
<td>1590 x 1590 microns, Area = 2.53 sq mm</td>
<td></td>
</tr>
<tr>
<td>BM-5 RumphCT</td>
<td>David Rumph</td>
<td>DMA controller</td>
<td>2442 x 2242 microns, Area = 5.47 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-12 TannerCT</td>
<td>John Tanner and Richard Segal</td>
<td>Single wire interface for a Manipulator (SWIM)</td>
<td>2000 x 3000 microns, Area = 6.00 sq mm</td>
<td></td>
</tr>
<tr>
<td>AG-1 WalpCT</td>
<td>Pat Walp</td>
<td>Array processor</td>
<td>2126 x 2050 microns, Area = 4.36 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-3 WatteyneCT</td>
<td>Thierry Watteyne and Martine Savalle</td>
<td>BCD/binary comparator</td>
<td>2100 x 1600 microns, Area = 3.36 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-11 WhitneyCT</td>
<td>Telle Whitney</td>
<td>Address translator</td>
<td>1940 x 2126 microns, Area = 4.12 sq mm</td>
<td></td>
</tr>
</tbody>
</table>
Carnegie-Mellon University:

[Summary of designs from CMU, updated 4-Dec-79 23:13:17]

AE-5 EbelingCMU  Designer: Carl Ebeling  
Description: Rebound Sorter  
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm

AE-1 GuptaCMU  Designer: Satish Gupta  
Description: Video Buffer  
Reserved space = 1006 x 5668 microns, Area = 5.70 sq mm

AE-8 HoeyCMU  Designer: Dan Hoey  
Description: Experimental Adder  
Reserved space = 1188 x 1976 microns, Area = 2.35 sq mm

AE-6 KungCMU  Designers: H. T. Kung, S. W. Song  
Description: Image Processing Chip  
Reserved space = 4160 x 2948 microns, Area = 12.26 sq mm

AE-7 SongCMU  Designer: Siang W Song  
Description: A small database machine  
Reserved space = 2224 x 1954 microns, Area = 4.35 sq mm

MIT:

[Summary of designs from MIT, updated 4-Dec-79 23:13:17]

AB-8 AllenMIT  Designers: Don Allen, Jerry Burchfiel  
Description: Variable Length Field Decoder  
Reserved space = 2218 x 2484 microns, Area = 5.51 sq mm

AB-1 BataliMIT  Designer: John Batali  
Description: Zero-Crossing Detector for Image Processing  
Reserved space = 2644 x 1738 microns, Area = 4.60 sq mm

AC-4 ChuMIT  Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick  
Description: Second order digital filter stage  
Reserved space = 6146 x 2278 microns, Area = 14.00 sq mm

AB-3 FichtenbaumMIT  Designer: Matt Fichtenbaum  
Description: A digital pulse rate monitor  
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm

AG-5 GoddeauMIT  Designers: David Goddeau, Jonathan Sieber, Chris Terman  
Description: A first-in, priority-out buffer  
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
MIT (cont.):

AB-5 GoodrichMIT  Designer: Earl Goodrich
   Description: CRT controller
   Reserved space = 1856 x 1520 microns, Area = 2.82 sq mm

AB-2 GramlichMIT  Designers: Wayne Gramlich, Carl Seaquist
   Description: A writable PLA in which the programming of the
   AND and OR planes is defined by contents of static RAM cells.
   Also can program feedback loops to form finite state machines.
   Reserved space = 1524 x 1906 microns, Area = 2.90 sq mm

AB-6 GrondalskiMIT Designer: Robert Grondalski
   Description: Writeable PLA
   Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm

AC-1 HamiltonMIT  Designer: Brian Hamilton
   Description: Digital Alarm Clock
   Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm

AG-2 KathailMIT    Designers: Vinod Kathail, Keshav Pingali
   Description: an interpreter for mapping programs onto
   a data flow computer
   Reserved space = 1590 x 2228 microns, Area = 3.54 sq mm

AB-4 KhouryMIT     Designer: John Khoury
   Description: Up-Down counter with programmable modulus
   Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm

AC-2 PasemanMIT    Designer: Bill Paseman
   Description: Music Synthesizer
   Reserved space = 4126 x 2842 microns, Area = 11.73 sq mm

AB-7 PicardMIT     Designer: Len Picard
   Description: Variable format field extractor and compactor
   Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm

AG-3 RivestMIT     Designers: Ron Rivest, Len Adleman, Adi Shamir
   Description: Section of a Multiplier
   Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
<table>
<thead>
<tr>
<th>Code</th>
<th>Designers</th>
<th>Description</th>
<th>Reserved space</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>BI-6</td>
<td>Atlas SU  Les Atlas, Doug Galbraith</td>
<td>This project is a neural-stim. interval timer</td>
<td>2478 x 1378 microns,</td>
<td>3.41 sq mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Area = 3.41 sq mm</td>
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</tr>
<tr>
<td>BK-4</td>
<td>Basket SU  Forest Baskett</td>
<td>This project is an Ethernet synchronizer</td>
<td>2240 x 2720 microns,</td>
<td>6.09 sq mm</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Area = 6.09 sq mm</td>
<td></td>
</tr>
<tr>
<td>BK-7</td>
<td>Bechtolsheim SU  Andy Bechtolsheim,</td>
<td>A parallel search table for log arithmetic</td>
<td>1514 x 3180 microns,</td>
<td>4.81 sq mm</td>
</tr>
<tr>
<td></td>
<td>Thomas Gross</td>
<td></td>
<td>Area = 4.81 sq mm</td>
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<tr>
<td>BK-5</td>
<td>Clark SU  Jim Clark</td>
<td>This project is a self-timed clock element</td>
<td>1606 x 1688 microns,</td>
<td>2.71 sq mm</td>
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<td></td>
<td></td>
<td></td>
<td>Area = 2.71 sq mm</td>
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<tr>
<td>BK-8</td>
<td>Clark SU  Jim Clark</td>
<td>This project is a simple graphics ALU</td>
<td>2976 x 2764 microns,</td>
<td>8.23 sq mm</td>
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<td>Area = 8.23 sq mm</td>
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<tr>
<td>BI-5</td>
<td>Elahian SU  Kamran Elahian, Fred Basham</td>
<td>This project is a UART line speed determiner</td>
<td>1856 x 1856 microns,</td>
<td>3.44 sq mm</td>
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<td>Area = 3.44 sq mm</td>
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</tr>
<tr>
<td>BK-3</td>
<td>Frolik SU  Bill Frolik, Roderick Young</td>
<td>This project is a digital timer</td>
<td>2120 x 2684 microns,</td>
<td>5.69 sq mm</td>
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<td></td>
<td>Area = 5.69 sq mm</td>
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<tr>
<td>BI-2</td>
<td>Gehlbach SU  Steve Gehlbach, Joe Sharp, Bill Jansen</td>
<td>This project is a fast 16-input adder</td>
<td>3180 x 1856 microns,</td>
<td>5.90 sq mm</td>
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<td>Area = 5.90 sq mm</td>
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<tr>
<td>BI-8</td>
<td>Hannah SU  Peter Eichenberger, Marc Hannah</td>
<td>This project is a rectangle generator</td>
<td>2386 x 2140 microns,</td>
<td>5.11 sq mm</td>
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<td>Area = 5.11 sq mm</td>
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</tr>
<tr>
<td>BI-7</td>
<td>Herndon SU  Matt Herndon, Jeff Thorson</td>
<td>This project is a typesetting machine</td>
<td>3170 x 2000 microns,</td>
<td>6.34 sq mm</td>
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<td>Area = 6.34 sq mm</td>
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<tr>
<td>BI-1</td>
<td>Macomber SU  Scott Macomber, Bob Clark</td>
<td>This project is a parallel/serial multiplier</td>
<td>2000 x 2000 microns,</td>
<td>4.00 sq mm</td>
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<td></td>
<td>Area = 4.00 sq mm</td>
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<tr>
<td>BI-3</td>
<td>Markee SU  Pat Markee, Irene Watson</td>
<td>This project is a digital clock</td>
<td>2120 x 1424 microns,</td>
<td>3.02 sq mm</td>
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<tr>
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<td></td>
<td></td>
<td>Area = 3.02 sq mm</td>
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</tbody>
</table>
BK-1 MathewsSU  Designers: Rob Mathews, John Newkirk
Description: This project is the infamous Buffalo chip
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm

BI-4 NoiceSU  Designers: David Noice, Neil Midkiff
Description: This project is a multiplier/divider
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm

BK-6 OhChinSU  Designers: Soo-Young Oh, Dae-Je Chin
Description: An automatic thermostat time controller
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm

BN-7 TarsiSU  Designers: Mike Tarsi, Nagatsugu Yamanouchi
Description: This project is a multifunction digital clock
Reserved space = 2140 x 2276 microns, Area = 4.87 sq mm

BN-6 UtsSU  Designers: Steve Uts, Shalom Ackelsberg
Description: This project is part of a pancreas prosthesis
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm

BI-9 WulffSU  Designers: Bob Wulff, Tom Bennett
Description: This project is a bit slice of a multiplier
Reserved space = 2120 x 1856 microns, Area = 3.93 sq mm

BK-2 ZarghanSU  Designers: Bahman Zargham, Jerry Huck
Description: This project is a multiplexed communications link
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm

U.C.Berkeley:

[Summary of designs from U.C.Berkeley, updated 4-Dec-79 23:13:17]

BM-2 DecuirUCB  Designers: J. Decuir, C.H. Sequin
Description: Sqaureoot of 3 approximator for radix-3 block in FFT computer
Reserved space = 2650 x 3278 microns, Area = 8.69 sq mm

BM-3 FungUCB  Designers: W.-C. Fung, C.H. Sequin
Description: General purpose barrel shifter for staggered, pipelined data in an FFT computer
Reserved space = 2484 x 2650 microns, Area = 6.58 sq mm

BM-4 LandmanUCB  Designer: Howard A. Landman
Description: This project is a reprogrammable PLA, with 8 each inputs, pterms, and (tri-state) outputs.
Reserved space = 2600 x 1590 microns, Area = 4.13 sq mm

BM-7 SequinUCB  Designer: Carlo H. Sequin
Description: Dual 16-stage FIFO with double rail signalling
Reserved space = 2460 x 980 microns, Area = 2.41 sq mm
Univ. of Illinois:

[Summary of designs from University of Illinois, updated 4-Dec-79 23:13:17]

AD-3 AdrianUI  Designers: Frank Adrian, Nick Fiduccia, Bud Pflug
Description: Functional equivalent of AMD 2901 ALU
to compare MOS, TTL
Reserved space = 2710 x 4388 microns, Area = 11.89 sq mm

AE-2 ClassUI  Designers: Class
Description: Twos complement 4 x 4 array multiplier
Reserved space = 1714 x 1498 microns, Area = 2.57 sq mm

AD-2 HanesUI  Designers: Larry Hanes, Dave Yen
Description: Twos complement array divider
Reserved space = 2616 x 2636 microns, Area = 6.90 sq mm

AD-1 LuhukayUI  Designer: Joe Luhukay
Description: Pipelined multiplier, registers also used for testability
Reserved space = 2572 x 4140 microns, Area = 10.65 sq mm

AD-4 MontoyeUI  Designers: Bob Montoye, Al Casavant
Description: Carry lookahead adder
(soln. proposed by Gajski and Kung)
Reserved space = 2628 x 2626 microns, Area = 6.90 sq mm

Univ. of Rochester:

[Summary of designs from University of Rochester, updated 4-Dec-79 23:13:17]

BN-3 KedemUR  Designers: Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Reserved space = 2698 x 2786 microns, Area = 7.52 sq mm

BN-2 LyonsUR  Designer: Bob Lyons
Description: Programmable Frequency Generator
Reserved space = 2748 x 2276 microns, Area = 6.25 sq mm

BN-4 SohmUR  Designers: Larry Sohm, Pat Chan, Bill Notowitz
Description: Digital Phase lock loop
Reserved space = 3610 x 2634 microns, Area = 9.51 sq mm

BN-5 TiloveUR  Designers: Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Reserved space = 1934 x 1326 microns, Area = 2.56 sq mm

BN-1 WatanabeUR  Designer: Yuki Watanabe
Description: Sorter slice
Reserved space = 2008 x 2240 microns, Area = 4.50 sq mm
Other places:

[Summary of designs from Other places, updated 4-Dec-79 23:13:17]

AC-3 GlasserOT
Designer: Lance Glasser, MIT, via Univ. of Washington
Description: Modulo-6 counter for dice game
Reserved space = 1486 x 808 microns, Area = 1.20 sq mm

AE-9 KehlOT
Designers: Ted Kehl, Ram Rao, Ed Lazowska,
Univ. of Washington, Seattle
Description: Address intercept logic for microcomputer
Reserved space = 1818 x 1782 microns, Area = 3.24 sq mm

AE-3 MurrayOT
Designer: John Murray, Univ. of Colorado, Colorado Springs,
via Univ. of Washington
Description: 3-bit identity comparator
Reserved space = 1512 x 1642 microns, Area = 2.48 sq mm

AE-4 RogersOT
Designer: Mike Rogers, Univ. of Bristol, Bristol, England,
via Univ. of Washington
Description: Simple 3-bit enciphering/deciphering chip.
Reserved space = 1248 x 1708 microns, Area = 2.13 sq mm

AF-1 Schip2
Designers: Gerry Sussman, Jack Holloway, Guy Steele, Alan Bell
MIT-AI Laboratory/Xerox PARC-SSL
Description: Lisp Microprocessor
Reserved space = 5926 x 7548 microns, Area = 44.73 sq mm

AG-4 SnyderOT
Designer: Larry Snyder, Yale University,
via University of Washington
Description: A binary tree processor that computes boolean functions, with inputs at the leaves and output at the root.
Reserved space = 3418 x 3430 microns, Area = 11.72 sq mm

AH-1 LhDoc1
Designer: Lynn Conway
Description: This is the Left Half of a "document chip",
describing MPC79, for use on MPC79A wafers.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm

BO-1 LhDoc2
This is the Left Half of the "document chip",
for use on MPC79B wafers.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm

AH-2 RHDoc1
Designer: Lynn Conway
Description: This is the Right Half of a "document chip",
flowcharting MPC79, for use on MPC79A wafers.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm

BO-2 RHDoc2
This is the Right Half of the "document chip",
for use on MPC79B wafers.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
MPG79: The demonstration of a prototype remote-entry, fast-turnaround, VLSI Implementation System

During the fall of 1979, the LSI Systems Area of Xerox PARC/SSL conducted the demonstration-operation of a prototype information management system, designed by Alan Bell and Martin Newell, for enabling the remote-entry, fast-turnaround implementation of large numbers of VLSI system designs. The user community for this demonstration was composed of EE/CS students taking courses in VLSI design at a number of universities, and university faculty and research staff members undertaking research prototype designs. MPG79 contains 75 designs submitted by 100 designers from many different universities.

The purposes of this effort were (i) to support the new university VLSI design courses by providing the implementation of student-project designs, (ii) to demonstrate the feasibility and general capabilities of such VLSI implementation systems to a wide technical community, and (iii) to refine our ideas about how to architect, design, and operate such systems by running a major operational test of a prototype system.

Several other organizations collaborated with us in conducting this demonstration: Data Communications (electronic messages and design file transfers) were supported by use of the ARPANET; maskmaking was done by Micro Mask, Inc., using an electron-beam mask-making system; wafer fabrication was done by Hewlett-Packard's Integrated Circuit Processing Laboratory.

The VLSI design techniques used in the university courses are described in the textbook Introduction to VLSI Systems, by C. Mead and L. Conway, Addison-Wesley publishing Co., 1980.

The background and context of the MPG79 effort, the structure of the MPG79 system, and the final results of the effort will be described in a Xerox PARC/SSL Report by L. Conway, A. Bell, and M. Newell entitled The Implementation of VLSI Systems.

The MPG79 Organizers:
Lynn Conway, Alan Bell, Martin Newell, Richard Lyon
LSI Systems Area, Xerox PARC/SSL
4 December 1979
To the MPC79 participants:

Melgar Photographers have recently taken photomicrographs of each of the die-types in the MPC79 Multiproject Chip Set. Prints of these photos can now be ordered by using the attached order form. The photos can be ordered in color, or in black and white, in standard sizes ranging from 5"x7" up to 20"x24". Prices as a function of size and type are listed on the order form. We can also make prints as large as 40"x60"! (Contact us for price quotes on sizes larger than 20"x24").

The order form indicates two further options:

(i) Full Die Photographs: Full Die Photographs include the Starting Frame, and all projects within the Starting Frame, for a given Die-Type. These can be ordered by Die-Code (AB, AC, - - -, etc.).

(ii) Individual Project Enlargements: These are produced using the original Full-Die negatives. Such enlargements of individual projects can be ordered by Project-Code (AB-1, AB-2, - - -, etc.).

A map of the MPC79 Die-Types, and a list of the Project-Codes and corresponding Project ID’s is given on the reverse side of this letter, for your convenience in determining the correct Die-Codes and Project-Codes for your order.

We will make the individual project enlargements at the quoted prices by using the original full-die negatives. This saves you from charges for rephotographing your individual project. In most cases, especially for the medium to large sized projects, this will yield good quality results. However, the smallest projects (for example AC-3) probably shouldn’t be enlarged to more than about 8"x10".

We can produce the highest quality photomicrographs of individual projects, especially the smaller ones, by rephotographing the wafers to obtain full-sized negatives containing only single, individual projects. We have some MPC79 wafers on file, and can arrange to rephotograph individual projects on a custom basis; please contact us to discuss prices and make arrangements for such custom work.

If you have any questions about the procedures for ordering MPC79 photos, or about prices, please feel free to phone me at (408) 733-4500.

Yours truly,

Frank Saude
President
ORDER FORM FOR MPC79 PHOTOGRAPHS:

To order photos of MPC79 Dies and/or individual Projects, complete this order form and mail to:

Melgar Photographers, 2971 Corvin Drive, Santa Clara, CA 95051.

Please make checks payable to Melgar Photographers. An example order is illustrated on the reverse side for your convenience. If you have any questions, contact Melgar at (408) 733-4500.

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Subtotal: ______________________

+ 6.5% Sales Tax if CA order: ______________________

+ 2.50 for postage and handling: 2.50

Final Total: ______________________
MPC79 Multiproject Chip Layouts
(with Die-Codes)

List of individual Project-Codes and corresponding Project ID's

**Wafer MPC79A**
- AB-1 RanaMIT
- AB-2 GreenshMIT
- AB-3 FeigenbaumMIT
- AB-4 KhouryMIT
- AB-5 GurvitzMIT
- AB-6 GrondahlMIT
- AB-7 PoonMIT
- AB-8 AllenMIT
- AC-1 HamiltonMIT
- AC-2 PariseauMIT
- AC-3 GuerarOT
- AC-4 ChuMIT
- AD-1 LubarskyUI
- AD-2 HarroUI
- AD-3 AdrianiUI
- AD-4 MontanyUI
- AE-1 GuptaCMU
- AE-2 ChuiUI
- AE-3 MutreyOT
- AE-4 RegenOT
- AE-5 EbelingCMU
- AF-1 KungCMU
- AF-2 SongCMU
- AF-3 HsuCMU
- AF-4 KehOT
- AF-5 Schip2
- AG-1 WalsCT
- AG-2 KshirMIT
- AG-3 RitenMIT
- AG-4 SnyderOT
- AG-5 GokhaneMIT

**Wafer MPC79B**
- BI-1 MaronberSU
- BI-2 GobbiSU
- BI-3 MarkesSU
- BI-4 NoizeSU
- BI-5 HuhBenSU
- BI-6 AtlasSU
- BI-7 HeninosSU
- BI-8 HannobSU
- BI-9 WolfSU
- BJ-1 CampbellCT
- BJ-2 FugCT
- BJ-3 PepsiCT
- BJ-4 LCT
- BJ-5 BartonCT
- BJ-6 CocomoCT
- BJ-7 PurcellCT
- BJ-8 RezatoCT
- BJ-9 KingsleyCT
- BJ-10 HsiCT
- BJ-11 WhitneyCT
- BJ-12 TannerCT
- BK-1 MathewSU
- BK-2 ZhangSU
- BK-3 FreiSU
- BK-4 TansSU
- BK-5 ClarkSU
- BK-6 DohlenSU
- BK-7 BarchalmSU
- BK-8 ClarkSU
- BL-1 HellingsCT
- BL-2 PatonCT
- BL-3 WatkinsCT
- BL-4 MitchellCT
- BL-5 GrantCT
- BL-6 PennCT
- BL-7 DerbyCT
- BL-8 PolemCT
- BM-1 LifickCT
- BM-2 DocciaUCB
- BM-3 FungUCB
- BM-4 LandmanUCB
- BM-5 KumpCT
- BM-6 ElicIT
- BM-7 SqueoUCB
- BN-1 WatanabeJR
- BN-2 LyonUR
- BN-3 KedemUR
- BN-4 SolbergUR
- BN-5 ThielJR
- BN-6 UshSU
- BN-7 TanSU
AN EXAMPLE COMPLETED ORDER FORM:

ORDER FORM FOR MPC79 PHOTOGRAPHS:

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<tr>
<td><strong>Name:</strong> Lynn Conway</td>
</tr>
<tr>
<td><strong>Address:</strong> 3333 Coyote Hill Rd.</td>
</tr>
<tr>
<td><strong>City:</strong> Palo Alto</td>
</tr>
<tr>
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</tr>
<tr>
<td><strong>ZIP:</strong> 94304</td>
</tr>
<tr>
<td><strong>Phone:</strong> (408) 494-4316</td>
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Full Die Photographs: (Please print Die-Code carefully; an example code: AB)

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Individual Project Enlargements: (print Project-Code carefully; example code: AB-8)

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Subtotal: 23.00
+ 6.5% Sales Tax if CA order: 1.50
+ $2.50 for postage and handling: 2.50
Final Total: 27.00

MELGAR NEGATIVE NUMBERS:
(for Melgar internal reference use)

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