List of Designers and their Projects

CALTECH:

[Summary of designs from CalTech, updated 4-Dec-79 23:13:17]

BJ-5 BartonCT
Designer: Eric Barton
Description: LED array driver
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm

BJ-8 BozzutoCT
Designer: Rick Bozzuto
Description: Pulse width to binary converter
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm

BJ-1 CampbellCT
Designer: James Campbell
Description: Logical processing unit with internal registers
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm

BJ-6 CocconiCT
Designer: Alan Cocconi
Description: Array processor
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm

BL-7 DerbyCT
Designer: Howard Derby
Description: Associative Memory
Reserved space = 2170 x 2566 microns, Area = 5.57 sq mm

BL-2 EatonCT
Designer: Steve Eaton
Description: Counter/adder
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm

BM-6 EllisCT
Designer: Mike Ellis
Description: Stepping motor controller
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm

BJ-2 FuCT
Designer: Sai Wai Fu
Description: Square root generator
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm

BL-5 GrayCT
Designer: Moshe Gray
Description: Array processor
Reserved space = 2534 x 2082 microns, Area = 5.28 sq mm

BL-1 HellerCT
Designer: Jack Heller
Description: Digital filter
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm

BJ-10 HoCT
Designer: Kuo Ting Ho
Description: 10 bit rate multiplier
Reserved space = 2120 x 1110 microns, Area = 2.35 sq mm

BJ-9 KingsleyCT
Designer: Chris Kingsley
Description: Serial Multiplier
Reserved space = 2200 x 2064 microns, Area = 4.54 sq mm
### CALTECH (cont.):

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<thead>
<tr>
<th>Design</th>
<th>Description</th>
<th>Designer(s)</th>
<th>Reserved space</th>
<th>Area</th>
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</thead>
<tbody>
<tr>
<td>BJ-4 LiCT</td>
<td>Two's-complement pipeline multiplier</td>
<td>Peggy Pey-Yun Li</td>
<td>2176 x 1326 microns, Area = 2.89 sq mm</td>
<td></td>
</tr>
<tr>
<td>BM-1 LigockiCT</td>
<td>Scan converter chip</td>
<td>Terry Ligocki</td>
<td>2000 x 4108 microns, Area = 8.22 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-4 MostellerCT</td>
<td>Stack-oriented microprocessor</td>
<td>Rick Mosteller, Greg Eflan, Dick Lang</td>
<td>4300 x 2996 microns, Area = 12.88 sq mm</td>
<td></td>
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<tr>
<td>BJ-3 PapachCT</td>
<td>Magnitude comparator</td>
<td>A.C. Papachristidis</td>
<td>2000 x 1126 microns, Area = 2.25 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-8 PedersenCT</td>
<td>Asynchronous FIFO</td>
<td>Bruce Pedersen</td>
<td>1896 x 2000 microns, Area = 3.79 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-6 PinesCT</td>
<td>Expandable clocking pattern generator chip</td>
<td>Elliot Pines</td>
<td>1780 x 1780 microns, Area = 3.17 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-7 PursifullCT</td>
<td>Self-Timed Queue</td>
<td>Ralph Pursiful</td>
<td>1590 x 1590 microns, Area = 2.53 sq mm</td>
<td></td>
</tr>
<tr>
<td>BM-5 RumphCT</td>
<td>DMA controller</td>
<td>David Rumph</td>
<td>2442 x 2242 microns, Area = 5.47 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-12 TannerCT</td>
<td>Single wire interface for a Manipulator (SWIM)</td>
<td>John Tanner and Richard Segal</td>
<td>2000 x 3000 microns, Area = 6.00 sq mm</td>
<td></td>
</tr>
<tr>
<td>AG-1 WalpCT</td>
<td>Array processor</td>
<td>Pat Walp</td>
<td>2126 x 2050 microns, Area = 4.36 sq mm</td>
<td></td>
</tr>
<tr>
<td>BL-3 WatteyneCT</td>
<td>BCD/binary comparator</td>
<td>Thierry Watteyne and Martine Savalle</td>
<td>2100 x 1600 microns, Area = 3.36 sq mm</td>
<td></td>
</tr>
<tr>
<td>BJ-11 WhitneyCT</td>
<td>Address translator</td>
<td>Telle Whitney</td>
<td>1940 x 2126 microns, Area = 4.12 sq mm</td>
<td></td>
</tr>
</tbody>
</table>
Carnegie-Mellon University:

[Summary of designs from CMU, updated 4-Dec-79 23:13:17]

AE-5 EbelingCMU
Designer: Carl Ebeling
Description: Rebound Sorter
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm

AE-1 GuptaCMU
Designer: Satish Gupta
Description: Video Buffer
Reserved space = 1006 x 5668 microns, Area = 5.70 sq mm

AE-8 HoeyCMU
Designer: Dan Hoey
Description: Experimental Adder
Reserved space = 1188 x 1976 microns, Area = 2.35 sq mm

AE-6 KungCMU
Designers: H. T. Kung, S. W. Song
Description: Image Processing Chip
Reserved space = 4160 x 2948 microns, Area = 12.26 sq mm

AE-7 SongCMU
Designer: Siang W Song
Description: A small database machine
Reserved space = 2224 x 1954 microns, Area = 4.35 sq mm

MIT:

[Summary of designs from MIT, updated 4-Dec-79 23:13:17]

AB-8 AllenMIT
Designers: Don Allen, Jerry Burchfiel
Description: Variable Length Field Decoder
Reserved space = 2218 x 2484 microns, Area = 5.51 sq mm

AB-1 BataliMIT
Designer: John Batali
Description: Zero-Crossing Detector for Image Processing
Reserved space = 2644 x 1738 microns, Area = 4.60 sq mm

AC-4 ChuMIT
Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick
Description: Second order digital filter stage
Reserved space = 6146 x 2278 microns, Area = 14.00 sq mm

AB-3 FichtenbaumMIT
Designer: Matt Fichtenbaum
Description: A digital pulse rate monitor
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm

AG-5 GoddeauMIT
Designers: David Goddeau, Jonathan Sieber, Chris Terman
Description: A first-in, priority-out buffer
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
MIT (cont.):

AB-5 GoodrichMIT  
Designer: Earl Goodrich  
Description: CRT controller  
Reserved space = 1856 x 1520 microns, Area = 2.82 sq mm

AB-2 GramlichMIT  
Designers: Wayne Gramlich, Carl Seaquist  
Description: A writable PLA in which the programming of the AND and OR planes is defined by contents of static RAM cells. Also can program feedback loops to form finite state machines.  
Reserved space = 1524 x 1906 microns, Area = 2.90 sq mm

AB-6 GrondalskiMIT  
Designer: Robert Grondalski  
Description: Writeable PLA  
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm

AC-1 HamiltonMIT  
Designer: Brian Hamilton  
Description: Digital Alarm Clock  
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm

AG-2 KathailMIT  
Designers: Vinod Kathail, Keshav Pingali  
Description: an interpreter for mapping programs onto a data flow computer  
Reserved space = 1590 x 2228 microns, Area = 3.54 sq mm

AB-4 KhouryMIT  
Designer: John Khoury  
Description: Up-Down counter with programmable modulus  
Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm

AC-2 PasemanMIT  
Designer: Bill Paseman  
Description: Music Synthesizer  
Reserved space = 4126 x 2842 microns, Area = 11.73 sq mm

AB-7 PicardMIT  
Designer: Len Picard  
Description: Variable format field extractor and compactor  
Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm

AG-3 RivestMIT  
Designers: Ron Rivest, Len Adleman, Adi Shamir  
Description: Section of a Multiplier  
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Stanford University:

[Summary of designs from Stanford University, updated 4-Dec-79 23:13:17]

BI-6 AtlasSU  Designers: Les Atlas, Doug Galbraith
Description: This project is a neural-stim. interval timer
Reserved space = 2478 x 1378 microns, Area = 3.41 sq mm

BK-4 BaskettSU  Designers: Forest Baskett
Description: This project is an Ethernet synchronizer
Reserved space = 2240 x 2720 microns, Area = 6.09 sq mm

BK-7 BechtolsheimSU  Designers: Andy Bechtolsheim, Thomas Gross
Description: A parallel search table for log arithmetic
Reserved space = 1514 x 3180 microns, Area = 4.81 sq mm

BK-5 Clark2SU  Designers: Jim Clark
Description: This project is a self-timed clock element
Reserved space = 1606 x 1688 microns, Area = 2.71 sq mm

BK-8 ClarkSU  Designers: Jim Clark
Description: This project is a simple graphics ALU
Reserved space = 2976 x 2764 microns, Area = 8.23 sq mm

BI-5 ElahianSU  Designers: Kamran Elahian, Fred Basham
Description: This project is a UART line speed determiner
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm

BK-3 FrolikSU  Designers: Bill Frolik, Roderick Young
Description: This project is a digital timer
Reserved space = 2120 x 2684 microns, Area = 5.69 sq mm

BI-2 GehlbachSU  Designers: Steve Gehlbach, Joe Sharp, Bill Jansen
Description: This project is a fast 16-input adder
Reserved space = 3180 x 1856 microns, Area = 5.90 sq mm

BI-8 HannahSU  Designers: Peter Eichenberger, Marc Hannah
Description: This project is a rectangle generator
Reserved space = 2386 x 2140 microns, Area = 5.11 sq mm

BI-7 HerndonSU  Designers: Matt Herndon, Jeff Thorson
Description: This project is a typesetting machine
Reserved space = 3170 x 2000 microns, Area = 6.34 sq mm

BI-1 MacomberSU  Designers: Scott Macomber, Bob Clark
Description: This project is a parallel/serial multiplier
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm

BI-3 MarkeeSU  Designers: Pat Markee, Irene Watson
Description: This project is a digital clock
Reserved space = 2120 x 1424 microns, Area = 3.02 sq mm
**BK-1 MathewsSU**  Designers: Rob Mathews, John Newkirk  
Description: This project is the infamous Buffalo chip  
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm

**BI-4 NoiceSU**  Designers: David Noice, Neil Midkiff  
Description: This project is a multiplier/divider  
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm

**BK-6 OhChinSU**  Designers: Soo-Young Oh, Dae-Je Chin  
Description: An automatic thermostat time controller  
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm

**BN-7 TarsiSU**  Designers: Mike Tarsi, Nagatsugu Yamanouchi  
Description: This project is a multifunction digital clock  
Reserved space = 2140 x 2276 microns, Area = 4.87 sq mm

**BN-6 UttSU**  Designers: Steve Utt, Shalom Ackelsberg  
Description: This project is part of a pancreas prosthesis  
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm

**BI-9 WulffSU**  Designers: Bob Wulff, Tom Bennett  
Description: This project is a bit slice of a multiplier  
Reserved space = 2120 x 1856 microns, Area = 3.93 sq mm

**BK-2 ZarghanSU**  Designers: Bahman Zargham, Jerry Huck  
Description: This project is a multiplexed communications link  
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm

**U.C.Berkeley:**

[Summary of designs from U.C.Berkeley, updated 4-Dec-79 23:13:17]
Univ. of Illinois:

[Summary of designs from University of Illinois, updated 4-Dec-79 23:13:17]

AD-3 AdrianUI  Designers: Frank Adrian, Nick Fiduccia, Bud Pflug
Description: Functional equivalent of AMD 2901 ALU
to compare MOS, TTL
Reserved space = 2710 x 4388 microns, Area = 11.89 sq mm

AE-2 ClassUI  Designers: Class
Description: Twos complement 4 x 4 array multiplier
Reserved space = 1714 x 1498 microns, Area = 2.57 sq mm

AD-2 HanesUI  Designers: Larry Hanes, Dave Yen
Description: Twos complement array divider
Reserved space = 2616 x 2636 microns, Area = 6.90 sq mm

AD-1 LuhukayUI  Designer: Joe Luhukay
Description: Pipelined multiplier, registers also used for testability
Reserved space = 2572 x 4140 microns, Area = 10.65 sq mm

AD-4 MontoyeUI  Designers: Bob Montoye, Al Casavant
Description: Carry lookahead adder
(soln. proposed by Gajski and Kung)
Reserved space = 2628 x 2626 microns, Area = 6.90 sq mm

Univ. of Rochester:

[Summary of designs from University of Rochester, updated 4-Dec-79 23:13:17]

BN-3 KedemUR  Designers: Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Reserved space = 2698 x 2786 microns, Area = 7.52 sq mm

BN-2 LyonsUR  Designer: Bob Lyons
Description: Programmable Frequency Generator
Reserved space = 2748 x 2276 microns, Area = 6.25 sq mm

BN-4 SohmUR  Designers: Larry Sohm, Pat Chan, Bill Notowitz
Description: Digital Phase lock loop
Reserved space = 3610 x 2634 microns, Area = 9.51 sq mm

BN-5 TiloveUR  Designers: Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Reserved space = 1934 x 1326 microns, Area = 2.56 sq mm

BN-1 WatanabeUR  Designer: Yuki Watanabe
Description: Sorter slice
Reserved space = 2008 x 2240 microns, Area = 4.50 sq mm
Other places:

[Summary of designs from Other places, updated 4-Dec-79 23:13:17]

**AC-3 GlasserOT**  
Designer: Lance Glasser, MIT, via Univ. of Washington  
Description: Modulo-6 counter for dice game  
Reserved space = 1486 x 808 microns, Area = 1.20 sq mm

**AE-9 KehlOT**  
Designers: Ted Kehl, Ram Rao, Ed Lazowska,  
Univ. of Washington, Seattle  
Description: Address intercept logic for microcomputer  
Reserved space = 1818 x 1782 microns, Area = 3.24 sq mm

**AE-3 MurrayOT**  
Designer: John Murray, Univ. of Colorado, Colorado Springs, via Univ. of Washington  
Description: 3-bit identity comparator  
Reserved space = 1512 x 1642 microns, Area = 2.48 sq mm

**AE-4 RogersOT**  
Designer: Mike Rogers, Univ. of Bristol, Bristol, England, via Univ. of Washington  
Description: Simple 3-bit enciphering/deciphering chip.  
Reserved space = 1248 x 1708 microns, Area = 2.13 sq mm

**AF-1 Schip2**  
Designers: Gerry Sussman, Jack Holloway, Guy Steele, Alan Bell  
MIT-AI Laboratory/Xerox PARC-SSL  
Description: Lisp Microprocessor  
Reserved space = 5926 x 7548 microns, Area = 44.73 sq mm

**AG-4 SnyderOT**  
Designer: Larry Snyder, Yale University, via University of Washington  
Description: A binary tree processor that computes boolean functions, with inputs at the leaves and output at the root.  
Reserved space = 3418 x 3430 microns, Area = 11.72 sq mm

**AH-1 LhDoc1**  
Designer: Lynn Conway  
Description: This is the Left Half of a "document chip", describing MPC79, for use on MPC79A wafers.  
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm

**BO-1 LhDoc2**  
This is the Left Half of the "document chip", for use on MPC79B wafers.  
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm

**AH-2 RHDoc1**  
Designer: Lynn Conway  
Description: This is the Right Half of a "document chip", flowcharting MPC79, for use on MPC79A wafers.  
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm

**BO-2 RHDoc2**  
This is the Right Half of the "document chip", for use on MPC79B wafers.  
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm