OTHER SUMMARY

6 proj.  65.50 mm²

(Doc chips not counted)

XEROX
Summary of designs from Other, updated 4-Dec-79 20:40:30

**Boyd0T**

Designer: David Boyd

Design is not ready for space allocation.
No file has been submitted for implementation.

**Glasser0T**

Designer: Lance Glasser

Design is awaiting allocation.
Required space = 1488 x 808 microns, Area = 1.20 sq mm
Priority time: 1-Dec-79 13:31:38
Current submittal is acceptable for implementation.
File name: [Max0]<LYON>GLASSER0T.CIF;1
File creation date: 1-Dec-79 13:31:38
Bounding box = 1488 x 808 microns, Area = 1.20 sq mm

**Keh0T**

Designer: Ted Kehl, Ram Rao, Ed Lazowska
Description: Address Intersect logic for microcomputer
Est. BB: 1815 X 1780 microns

Design is awaiting allocation.
Required space = 1815 x 1782 microns, Area = 3.24 sq mm
Priority time: 24-Nov-79 12:28:02
Current submittal is acceptable for implementation.
File name: [Max0]<LYON>XEHLOT.CIF;1
File creation date: 24-Nov-79 12:28:02
Bounding box = 1815 x 1782 microns, Area = 3.24 sq mm

**LD0C1**

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Max0]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

**LD0C2**

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Max0]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

**Murray0T**

Designer: John Murray

Design is awaiting allocation.
Required space = 1512 x 1642 microns, Area = 2.48 sq mm
Priority time: 3-Dec-79 11:40:27
Current submittal is acceptable for implementation.
File name: [Max0]<LYON>MURRAY0T.CIF;1
File creation date: 3-Dec-79 11:40:27
Bounding box = 1512 x 1642 microns, Area = 2.48 sq mm
This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

Design: Mike Rodgers

Design is awaiting allocation.
Required space = 1248 x 1708 microns, Area = 2.13 sq mm
Priority time: 3-Dec-79 13:12:01
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>RODGERSDT.CIF;3
File creation date: 3-Dec-79 13:12:01
Bounding box = 1248 x 1708 microns, Area = 2.13 sq mm

Designers: Gerry Sussman, Jack Holloway, Guy Steele, Alan Bell
Description: LISP Microprocessor
Est.BB: 7548 x 5925 microns

Space is allocated.
Reserved space = 5925 x 7548 microns, Area = 44.73 sq mm
Priority time: 19-Nov-79 21:25:06
Current submittal is acceptable for implementation.
File name: [Maxc]<ADELL>SCHIP2C.CIF;1
File creation date: 19-Nov-79 21:25:06
Bounding box = 5925 x 7548 microns, Area = 44.73 sq mm

Design is not ready for space allocation.
No file has been submitted for implementation.

Designer(s): Lee Smith, Irene Buchanan
Description: Link Design
Est.BB: ~ 2000 X 1400 microns.

Design is awaiting allocation.
Required space = 3418 x 3430 microns, Area = 11.72 sq mm
Priority time: 27-Nov-79 18:49:56
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>SHYDEROT.CIF.
File creation date: 3-Dec-79 11:23:20
Bounding box = 3418 x 3430 microns, Area = 11.72 sq mm