Memo from: LYNN CONWAY

What happened to Me.Doc ?

~CALTECH SUMMARY

~~22~~ 23 proj.	94.28 mm^2

+ HIT LIST :

1 proj.	9.83 mm^2

XEROX

CALTECH FINAL

Summary of designs from CalTech, updated 4-Dec-79 22:28:11

✔ BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:35
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

✔ BozzutoCT

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

✔ CampbellCT

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

✔ CocconiCT

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;3
File creation date: 4-Dec-79 15:02:38
Bounding box = 1896 x 1074 microns, Area = 2.04 sq mm

✔ DerbyCT

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;4
File creation date: 4-Dec-79 15:04:56
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

✔ EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

✔ EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

✔ FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

✔ GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2082 microns, Area = 5.28 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;4
File creation date: 4-Dec-79 15:08:13
Bounding box = 2534 x 2082 microns, Area = 5.28 sq mm

✔ HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

✓ HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

✓ KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2064 microns, Area = 4.54 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;3
File creation date: 4-Dec-79 15:03:33
Bounding box = 2200 x 2064 microns, Area = 4.54 sq mm

✓ LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

✓ LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Design is awaiting allocation.
Required space = 2000 x 4108 microns, Area = 8.22 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;3
File creation date: 4-Dec-79 15:11:59
Bounding box = 2000 x 4108 microns, Area = 8.22 sq mm

✓ MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;3
File creation date: 4-Dec-79 15:09:38
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

✓ PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

✓ PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;3
File creation date: 4-Dec-79 15:03:17
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

✓ PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

✓ PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;3
File creation date: 4-Dec-79 15:09:25
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

✓ RumphCT HIT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

Design is awaiting allocation.
Required space = 2442 x 2242 microns, Area = 5.47 sq mm
Priority time: 27-Nov-79 17:42:58
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 4-Dec-79 13:24:20
Bounding box = 2442 x 2242 microns, Area = 5.47 sq mm

✓ TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;3
File creation date: 4-Dec-79 15:06:17
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT [redacted] → went onto MIT3.

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;3
File creation date: 4-Dec-79 15:08:49
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

✓ WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

✓ WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;3
File creation date: 4-Dec-79 15:12:25
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH

Summary of designs from CalTech, updated 4-Dec-79 3:51:33

BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

;2

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:36
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

BozzutoCT

;1

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

CampbellCT

2

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

CocconiCT

;3

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;2
File creation date: 3-Dec-79 23:25:26

DerbyCT

;4

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;2
File creation date: 3-Dec-79 23:34:54
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2152 microns, Area = 5.45 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;2
File creation date: 3-Dec-79 23:43:51
Bounding box = 2534 x 2152 microns, Area = 5.45 sq mm

HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;2
File creation date: 3-Dec-79 23:31:16

LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;2
File creation date: 3-Dec-79 23:53:54

MartinCT

Designer(s): Kreg Martin
Description: Serial Array processing element
Est.BB: ~2000 x 2375 microns

Design is awaiting allocation.
Required space = 2376 x 2126 microns, Area = 5.05 sq mm
Priority time: 1-Dec-79 18:49:01
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MARTINCT.CIF;2
File creation date: 3-Dec-79 23:40:55
Bounding box = 2376 x 2126 microns, Area = 5.05 sq mm

MeadorCT

Designer(s): Jim Meador
Description: 4-digit clock chip
Est.BB: ~2100 x 1800 microns

Space is allocated.
Reserved space = 2000 x 2388 microns, Area = 4.78 sq mm
Priority time: 1-Dec-79 20:29:19
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MEADORCT.CIF;4
File creation date: 1-Dec-79 20:29:19
Bounding box = 2000 x 2388 microns, Area = 4.78 sq mm

MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;2
File creation date: 3-Dec-79 23:50:32
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;2
File creation date: 3-Dec-79 23:30:23
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;2
File creation date: 3-Dec-79 23:49:37
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

RumphCT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

;1

Design is not ready for space allocation.
Current submittal checked ok.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 27-Nov-79 17:42:58
Bounding box = 1002 x 1130 microns, Area = 1.13 sq mm

ShahCT

~~Designer(s): Deepak Shah~~
~~Description: Array processor~~
~~Est.BB: ~2250 x 2250 microns~~

DEL

Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 26-Nov-79 23:50:18
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>SHAHCT.CIF;2
File creation date: 3-Dec-79 23:32:11
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm

TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

;3

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;2
File creation date: 3-Dec-79 23:39:02
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

;3

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;2
File creation date: 3-Dec-79 23:47:47
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

;2

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

13

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;2
File creation date: 3-Dec-79 23:54:52
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH PRIORITIES

(1) Mosteller, Tanner, Whitney, Barton
Derby, Li, Ligocki

(2) (all the rest)

(3) ? Cocconi ?

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(4) Walp, Meador, Rumph

↓ HIT