MPC79 University Merges:

Memo from: LYNN CONWAY

UCB SUMMARY

4 proj.	21.81 mm^2

XEROX

Summary of designs from UCB, updated 4-Dec-79 20:40:30

✔DecuirUCB

Designers: J. Decuir, C.H.Sequin
Description: squareroot of 3 approximator for
radix-3 block in FFT computer
BOUNDS: 265000 327750 132500,163875

Design is awaiting allocation.
Required space = 2650 x 3278 microns, Area = 8.69 sq mm
Priority time: 4-Dec-79 13:13:22
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>DECUIRUCB.;2
File creation date: 4-Dec-79 13:13:22
Bounding box = 2650 x 3278 microns, Area = 8.69 sq mm

✔FungUCB

Designers: W.-C. Fung, C.H.Sequin
Description: general purpose barrel shifter for sraggered ,
pipelined data in an FFT computer
BOUNDS: B 248250 265000 124125,132500

Design is awaiting allocation.
Required space = 2484 x 2650 microns, Area = 6.58 sq mm
Priority time: 3-Dec-79 20:30:14
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>FUNGUCB.;2
File creation date: 3-Dec-79 20:30:14
Bounding box = 2484 x 2650 microns, Area = 6.58 sq mm

✔LandmanUCB

Designer: Howard A. Landman
Description: This project is a reprogrammable PLA, with
8 each inputs, pterms, and (tri-state) outputs.
Est.BB: ~2600 x 1600 microns

Design is awaiting allocation.
Required space = 2600 x 1590 microns, Area = 4.13 sq mm
Priority time: 3-Dec-79 12:20:29
Current submittal is acceptable for implementation.
File name: [Maxc]<LANDMAN>MPC79-LANDMANUCB.CIF;1
File creation date: 3-Dec-79 12:20:29
Bounding box = 2600 x 1590 microns, Area = 4.13 sq mm

✔SequinUCB

Designer Carlo H. Sequin
Description: Dual 16-stage FIFO with double rail signalling
Est BB: 2460 980

Space is allocated.
Reserved space = 2460 x 980 microns, Area = 2.41 sq mm
Priority time: 5-Nov-79 10:47:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SEQUIN>SEQUINUCB.CIF;1
File creation date: 5-Nov-79 10:47:48
Bounding box = 2460 x 980 microns, Area = 2.41 sq mm

Memo from: LYNN CONWAY

What happened to Me.Doc ?

~CALTECH SUMMARY

~~22~~ 23 proj.	94.28 mm^2

+ HIT LIST :

1 proj.	9.83 mm^2

XEROX

CALTECH FINAL

Summary of designs from CalTech, updated 4-Dec-79 22:28:11

✔ BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:35
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

✔ BozzutoCT

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

✔ CampbellCT

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

✔ CocconiCT

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;3
File creation date: 4-Dec-79 15:02:38
Bounding box = 1896 x 1074 microns, Area = 2.04 sq mm

✔ DerbyCT

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;4
File creation date: 4-Dec-79 15:04:56
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

✔ EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

✔ EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

✔ FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

✔ GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2082 microns, Area = 5.28 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;4
File creation date: 4-Dec-79 15:08:13
Bounding box = 2534 x 2082 microns, Area = 5.28 sq mm

✔ HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

✓ HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

✓ KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2064 microns, Area = 4.54 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;3
File creation date: 4-Dec-79 15:03:33
Bounding box = 2200 x 2064 microns, Area = 4.54 sq mm

✓ LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

✓ LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Design is awaiting allocation.
Required space = 2000 x 4108 microns, Area = 8.22 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;3
File creation date: 4-Dec-79 15:11:59
Bounding box = 2000 x 4108 microns, Area = 8.22 sq mm

✓ MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;3
File creation date: 4-Dec-79 15:09:38
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

✓ PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

✓ PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;3
File creation date: 4-Dec-79 15:03:17
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

✓ PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

✓ PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;3
File creation date: 4-Dec-79 15:09:25
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

✓ RumphCT HIT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

Design is awaiting allocation.
Required space = 2442 x 2242 microns, Area = 5.47 sq mm
Priority time: 27-Nov-79 17:42:58
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 4-Dec-79 13:24:20
Bounding box = 2442 x 2242 microns, Area = 5.47 sq mm

✓ TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;3
File creation date: 4-Dec-79 15:06:17
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT [redacted] → went onto MIT3.

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;3
File creation date: 4-Dec-79 15:08:49
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

✓ WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

✓ WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;3
File creation date: 4-Dec-79 15:12:25
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH

Summary of designs from CalTech, updated 4-Dec-79 3:51:33

BartonCT

Designer(s): Eric Barton
Description: LED array driver
Est.BB: ~2125 x 2125 microns

;2

Space is allocated.
Reserved space = 2126 x 2126 microns, Area = 4.52 sq mm
Priority time: 26-Nov-79 22:33:36
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BARTONCT.CIF;2
File creation date: 3-Dec-79 23:33:26
Bounding box = 2126 x 2126 microns, Area = 4.52 sq mm

BozzutoCT

;1

Designer(s): Rick Bozzuto
Description: Pulse width to binary converter
Est.BB: ~1500 x 2300 microns

Space is allocated.
Reserved space = 2120 x 1288 microns, Area = 2.73 sq mm
Priority time: 26-Nov-79 22:35:51
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>BOZZUTOCT.CIF;1
File creation date: 3-Dec-79 23:51:28
Bounding box = 2120 x 1288 microns, Area = 2.73 sq mm

CampbellCT

2

Designer(s): James Campbel
Description: Logical processing unit with internal registers
Est.BB: ~1400 X 1400 microns

Space is allocated.
Reserved space = 1856 x 1704 microns, Area = 3.16 sq mm
Priority time: 27-Nov-79 0:03:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>CAMPBELLCT.CIF;2
File creation date: 3-Dec-79 23:38:10
Bounding box = 1856 x 1704 microns, Area = 3.16 sq mm

CocconiCT

;3

Designer: Alan Cocconi
Description: array processor
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1896 x 1074 microns, Area = 2.04 sq mm
Priority time: 1-Dec-79 20:20:33
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>COCCONICT.CIF;2
File creation date: 3-Dec-79 23:25:26

DerbyCT

;4

Designer(s): Howard Derby
Description: Associative Memory
Est.BB: ~2250 x 2250 microns

Design is awaiting allocation.
Required space = 2170 x 2566 microns, Area = 5.57 sq mm
Priority time: 26-Nov-79 22:39:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>DERBYCT.CIF;2
File creation date: 3-Dec-79 23:34:54
Bounding box = 2170 x 2566 microns, Area = 5.57 sq mm

EatonCT

Designer(s): Steve Eaton
Description: Counter/adder
Est.BB: ~ 1400 x 2600 microns

Space is allocated.
Reserved space = 2500 x 1376 microns, Area = 3.44 sq mm
Priority time: 26-Nov-79 23:14:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>EATONCT.CIF;2
File creation date: 3-Dec-79 23:53:13
Bounding box = 2500 x 1376 microns, Area = 3.44 sq mm

EllisCT

Designer(s): Mike Ellis
Description: Stepping motor controller
Est.BB: ~2125 microns x 2000 microns

Space is allocated.
Reserved space = 2000 x 2500 microns, Area = 5.00 sq mm
Priority time: 26-Nov-79 23:18:09
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>ELLISCT.CIF;2
File creation date: 3-Dec-79 23:42:35
Bounding box = 2000 x 2500 microns, Area = 5.00 sq mm

FuCT

Designer(s): Sai Wai Fu
Description: Square root generator
Est.BB: ~1600 x 1900 microns

Space is allocated.
Reserved space = 1750 x 1626 microns, Area = 2.85 sq mm
Priority time: 1-Dec-79 13:34:10
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>FUCT.CIF;2
File creation date: 3-Dec-79 23:52:32
Bounding box = 1750 x 1626 microns, Area = 2.85 sq mm

GrayCT

Designer(s): Moshe Gray
Description: Array processor
Est.BB: ~1900 x 1900 microns

Design is awaiting allocation.
Required space = 2534 x 2152 microns, Area = 5.45 sq mm
Priority time: 26-Nov-79 23:27:57
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>GRAYCT.CIF;2
File creation date: 3-Dec-79 23:43:51
Bounding box = 2534 x 2152 microns, Area = 5.45 sq mm

HellerCT

Designer(s): Jack Heller
Description: Digital filter
Est.BB: ~2000 x 2000 microns

Space is allocated.
Reserved space = 2708 x 1326 microns, Area = 3.59 sq mm
Priority time: 26-Nov-79 23:29:12
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HELLERCT.CIF;2
File creation date: 3-Dec-79 23:39:56
Bounding box = 2708 x 1326 microns, Area = 3.59 sq mm

HoCT

Designer(s): Kuo Ting Ho
Description: 10 bit rate multipler
Est.BB: ~1000 x 1700 microns

Design is awaiting allocation.
Required space = 2120 x 1110 microns, Area = 2.35 sq mm
Priority time: 26-Nov-79 23:30:45
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>HOCT.CIF;2
File creation date: 3-Dec-79 23:41:41
Bounding box = 2120 x 1110 microns, Area = 2.35 sq mm

KingsleyCT

Designer(s): Chris Kingsley
Description: Serial Multipler
Est.BB: ~2200 microns x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 26-Nov-79 23:32:05
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>KINGSLEYCT.CIF;2
File creation date: 3-Dec-79 23:31:16

LiCT

Designer(s): Peggy Pey-Yun Li
Description: Two's-complement pipeline multiplier
Est.BB: ~1200 x 1700 microns

Space is allocated.
Reserved space = 2176 x 1326 microns, Area = 2.89 sq mm
Priority time: 26-Nov-79 23:33:15
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>LICT.CIF;2
File creation date: 3-Dec-79 23:48:33
Bounding box = 2176 x 1326 microns, Area = 2.89 sq mm

LigockiCT

Designer(s): Terry Ligocki
Description: Scan converter chip
Est.BB: ~2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 26-Nov-79 23:34:29
Current submittal is not implementable.
File name: [Maxc]<CALTECH-VLSI>LIGOCKICT.CIF;2
File creation date: 3-Dec-79 23:53:54

MartinCT

Designer(s): Kreg Martin
Description: Serial Array processing element
Est.BB: ~2000 x 2375 microns

Design is awaiting allocation.
Required space = 2376 x 2126 microns, Area = 5.05 sq mm
Priority time: 1-Dec-79 18:49:01
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MARTINCT.CIF;2
File creation date: 3-Dec-79 23:40:55
Bounding box = 2376 x 2126 microns, Area = 5.05 sq mm

MeadorCT

Designer(s): Jim Meador
Description: 4-digit clock chip
Est.BB: ~2100 x 1800 microns

Space is allocated.
Reserved space = 2000 x 2388 microns, Area = 4.78 sq mm
Priority time: 1-Dec-79 20:29:19
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MEADORCT.CIF;4
File creation date: 1-Dec-79 20:29:19
Bounding box = 2000 x 2388 microns, Area = 4.78 sq mm

MostellerCT

Designer(s): Rick Mosteller, Greg Eflan, DIck Lang
Description: Stack-oriented micrprocessor
EstBB: 6000 x 4000 microns

Space is allocated.
Reserved space = 4300 x 2996 microns, Area = 12.88 sq mm
Priority time: 30-Nov-79 17:46:53
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>MOSTELLERCT.CIF;2
File creation date: 3-Dec-79 23:50:32
Bounding box = 4300 x 2996 microns, Area = 12.88 sq mm

PapachCT

Designer(s): A.C. Papachristidis
Description: Magnitude comparator
Est.BB: ~2100 x 1200 microns

Space is allocated.
Reserved space = 2000 x 1126 microns, Area = 2.25 sq mm
Priority time: 26-Nov-79 23:41:40
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PAPACHCT.CIF;2
File creation date: 3-Dec-79 23:29:15
Bounding box = 2000 x 1126 microns, Area = 2.25 sq mm

PedersenCT

Designer(s): Bruce Pedersen
Description: Asynchronous FIFO
Est.BB: ~ 2000 microns x 2000 microns

Design is awaiting allocation.
Required space = 1896 x 2000 microns, Area = 3.79 sq mm
Priority time: 26-Nov-79 23:43:30
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PEDERSENCT.CIF;2
File creation date: 3-Dec-79 23:30:23
Bounding box = 1896 x 2000 microns, Area = 3.79 sq mm

PinesCT

Designer(s): Elliot Pines
Description: Expandable clocking pattern generator chip
Est.BB: ~1800 x 1800 microns

Space is allocated.
Reserved space = 1780 x 1780 microns, Area = 3.17 sq mm
Priority time: 26-Nov-79 23:48:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PINESCT.CIF;2
File creation date: 3-Dec-79 23:34:06
Bounding box = 1780 x 1780 microns, Area = 3.17 sq mm

PursifullCT

Designer(s): Ralph Pursiful
Description: Self-Timed Queue
Est.BB: ~2300 X 2300 microns

Space is allocated.
Reserved space = 1590 x 1590 microns, Area = 2.53 sq mm
Priority time: 27-Nov-79 0:02:06
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>PURSIFULLCT.CIF;2
File creation date: 3-Dec-79 23:49:37
Bounding box = 1590 x 1590 microns, Area = 2.53 sq mm

RumphCT

Designer(s): David Rumph
Description: DMA controller
Est.BB: ~2000 x 2000 microns

;1

Design is not ready for space allocation.
Current submittal checked ok.
File name: [Maxc]<CALTECH-VLSI>RUMPHCT.CIF;1
File creation date: 27-Nov-79 17:42:58
Bounding box = 1002 x 1130 microns, Area = 1.13 sq mm

ShahCT

~~Designer(s): Deepak Shah~~
~~Description: Array processor~~
~~Est.BB: ~2250 x 2250 microns~~

DEL

Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 26-Nov-79 23:50:18
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>SHAHCT.CIF;2
File creation date: 3-Dec-79 23:32:11
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm

TannerCT

Designer(s): John Tanner and Richard Segal
Description: Single wire interface for a Manipulator (SWIM)
Est.BB: ~3200 x 2200 microns

;3

Space is allocated.
Reserved space = 2000 x 3000 microns, Area = 6.00 sq mm
Priority time: 26-Nov-79 23:57:37
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>TANNERCT.CIF;2
File creation date: 3-Dec-79 23:39:02
Bounding box = 2000 x 3000 microns, Area = 6.00 sq mm

WalpCT

Designer(s): Pat Walp
Description: array processor
Est.BB: ~2200 x 2000 microns

;3

Design is awaiting allocation.
Required space = 2126 x 2050 microns, Area = 4.36 sq mm
Priority time: 3-Dec-79 23:47:47
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WALPCT.CIF;2
File creation date: 3-Dec-79 23:47:47
Bounding box = 2126 x 2050 microns, Area = 4.36 sq mm

WatteyneCT

Designer(s): Thierry Watteyne and Martine Savalle
Description: BCD/binary comparator
Est.BB: ~ 2100 microns x 1600 microns

;2

Space is allocated.
Reserved space = 2100 x 1600 microns, Area = 3.36 sq mm
Priority time: 26-Nov-79 23:59:25
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WATTEYNECT.CIF;2
File creation date: 3-Dec-79 23:44:39
Bounding box = 2100 x 1600 microns, Area = 3.36 sq mm

WhitneyCT

Designer(s): Telle Whitney
Description: Address translator
Est.BB: ~2000 x 2000 microns

13

Space is allocated.
Reserved space = 1940 x 2126 microns, Area = 4.12 sq mm
Priority time: 27-Nov-79 0:01:04
Current submittal is acceptable for implementation.
File name: [Maxc]<CALTECH-VLSI>WHITNEYCT.CIF;2
File creation date: 3-Dec-79 23:54:52
Bounding box = 1940 x 2126 microns, Area = 4.12 sq mm

CALTECH PRIORITIES

(1) Mosteller, Tanner, Whitney, Barton
Derby, Li, Ligocki

(2) (all the rest)

(3) ? Cocconi ?

---

(4) Walp, Meador, Rumph

↓ HIT

Memo from: LYNN CONWAY

CMU SUMMARY

5 proj.	28.10 mm^2

XEROX

CMU FINAL

Summary of designs from CMU, updated 4-Dec-79 22:28:11

EbelingCMU

Designer: Carl Ebeling
Description: Rebound Sorter
Est.BB: 2000 X 2000 microns

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 27-Nov-79 8:04:24
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>EBELINGCMU.CIF;2
File creation date: 4-Dec-79 8:15:59
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

GuptaCMU

Designer: Satish Gupta
Description: Video Buffer
Est.BB: 5000 X 1000 microns

Space is allocated.
Reserved space = 1006 x 5668 microns, Area = 5.70 sq mm
Priority time: 27-Nov-79 17:22:44
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>GUPTACMU.CIF;2
File creation date: 1-Dec-79 13:53:57
Bounding box = 1006 x 5668 microns, Area = 5.70 sq mm

HoeyCMU

Designer: Dan Hoey
Description: Experimental Adder
EstBB: 4000 x 4000 microns

Space is allocated.
Reserved space = 1188 x 1976 microns, Area = 2.35 sq mm
Priority time: 27-Nov-79 17:23:54
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>HOEYCMU.CIF;4
File creation date: 3-Dec-79 9:36:41
Bounding box = 1188 x 1976 microns, Area = 2.35 sq mm

KungCMU

Designer: H. T. Kung, S. W. Song
Description: Image Processing Chip
Est.BB: 3500 X 2300 microns

Design is awaiting allocation.
Required space = 4160 x 2948 microns, Area = 12.26 sq mm
Priority time: 1-Dec-79 11:29:02
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>KUNGCMU.CIF;8
File creation date: 4-Dec-79 21:28:30
Bounding box = 4160 x 2948 microns, Area = 12.26 sq mm

SongCMU

Designer: Siang W Song
Description: A small database machine
Est.BB: 2000 X 2000 microns

Space is allocated.
Reserved space = 2224 x 1954 microns, Area = 4.35 sq mm
Priority time: 27-Nov-79 8:54:16
Current submittal is acceptable for implementation.
File name: [Maxc]<CMU-VLSI>SONGCMU.CIF;5

File creation date: 4-Dec-79 15:05:14
Bounding box = 2224 x 1954 microns, Area = 4.35 sq mm

Memo from: LYNN CONWAY

ILLINOIS SUMMARY

5 proj.	38.91 mm^2

XEROX

ILLINOIS FINAL

Summary of designs from Illinois, updated 4-Dec-79 20:40:30

✓ AdrianUI

Designers: Frank Adrian, Nick Fiduccia, Bud Pflug
Description: Functional equivalent of AMD 2901 ALU to compare MOS, TTL
Est.BB: ~ 2000 X 2000 microns

Space is allocated.
Reserved space = 2710 x 4388 microns, Area = 11.89 sq mm
Priority time: 27-Nov-79 15:23:08
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>ADRIANUI.CIF;3
File creation date: 4-Dec-79 13:24:09
Bounding box = 2710 x 4388 microns, Area = 11.89 sq mm

✓ ClassUI

Designers: Class
Description: Twos complement 4 x 4 array multiplier
Est.BB: 1200 x 1200

Space is allocated.
Reserved space = 1714 x 1498 microns, Area = 2.57 sq mm
Priority time: 27-Nov-79 11:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>CLASSUI.CIF;3
File creation date: 3-Dec-79 13:54:59
Bounding box = 1714 x 1498 microns, Area = 2.57 sq mm

✓ HanesUI

Designers: Larry Hanes, Dave Yen
Description: Twos complement array divider
Est.BB: ~ 2000 X 2000 microns

Space is allocated.
Reserved space = 2616 x 2636 microns, Area = 6.90 sq mm
Priority time: 27-Nov-79 15:00:02
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>HANESUI.CIF;3
File creation date: 3-Dec-79 21:33:23
Bounding box = 2616 x 2636 microns, Area = 6.90 sq mm

✓ LuhukayUI

Designer: Joe Luhukay
Description: Pipelined multiplier, registers also used for testability
Est.BB: ~ 2000 X 1250 microns

Design is awaiting allocation.
Required space = 2572 x 4140 microns, Area = 10.65 sq mm
Priority time: 22-Nov-79 21:26:35
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>LUHUKAYUI.CIF;3
File creation date: 4-Dec-79 7:21:44
Bounding box = 2572 x 4140 microns, Area = 10.65 sq mm

✓ MontoyeUI

Designers: Bob Montoye, Al Casavant
Description: Carry lookahead adder (soln. proposed by Gajski and Kung)
Est.BB: ~ 2000 X 1500 microns.

Design is awaiting allocation.
Required space = 2628 x 2626 microns, Area = 6.90 sq mm
Priority time: 27-Nov-79 8:33:59
Current submittal is acceptable for implementation.
File name: [Maxc]<ILLINOIS-VLSI>MONTOYEUI.CIF;2
File creation date: 4-Dec-79 13:28:21
Bounding box = 2628 x 2626 microns, Area = 6.90 sq mm

Memo from: LYNN CONWAY

MIT

SUMMARY:

~~15~~ 14 proj.	91.23 mm²

XEROX

MIT FINAL

Summary of designs from MIT, updated 4-Dec-79 19:02:23

✓AllenMIT

Designers: Don Allen, Jerry Burchfiel
Description: Variable Length Field Decoder
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2218 x 2484 microns, Area = 5.51 sq mm
Priority time: 28-Nov-79 7:45:20
Current submittal is acceptable for implementation.
File name: [Maxc]<ABELL>ALLENMIT.CIF;3
File creation date: 4-Dec-79 18:44:50
Bounding box = 2218 x 2484 microns, Area = 5.51 sq mm

✓BataliMIT

Designers: John Batali
Description: Zero-Crossing Detector for Image Processing
Est.BB 2650 x 1575

Design is awaiting allocation.
Required space = 2644 x 1738 microns, Area = 4.60 sq mm
Priority time: 29-Nov-79 5:59:14
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BATALIMIT.CIF;3
File creation date: 4-Dec-79 16:35:08
Bounding box = 2644 x 1738 microns, Area = 4.60 sq mm

BodonyMIT

Designers: Larry Bodony, Bruce Rose
Description: Logic State Analyzer
Est.BB: 4500 x 2650 microns

Design is awaiting allocation.
Required space = 4500 x 4336 microns, Area = 19.51 sq mm
Priority time: 28-Nov-79 7:45:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BODONYMIT.CIF;2
File creation date: 4-Dec-79 16:55:27
Bounding box = 4500 x 4336 microns, Area = 19.51 sq mm

ChangMIT

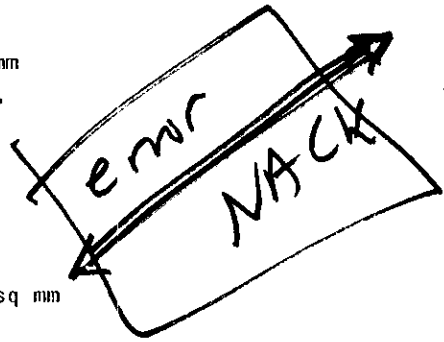
Designers: Frank Chang, Doug Williams
Description: Error-detecting block transfer oriented channel interface
Est.BB: 2500 x 5250 microns

Space is allocated.
Reserved space = 2764 x 2500 microns, Area = 6.91 sq mm
Priority time: 29-Nov-79 5:59:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHANGMIT.CIF;4
File creation date: 4-Dec-79 16:17:37
Bounding box = 2764 x 2500 microns, Area = 6.91 sq mm

✓ChuMIT

Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick
Description: Second order digital filter stage
Est.BB: 2400 x 6200 microns

Space is allocated.
Reserved space = 6146 x 2278 microns, Area = 14.00 sq mm
Priority time: 29-Nov-79 6:00:45
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHUMIT.CIF;3
File creation date: 4-Dec-79 13:47:06
Bounding box = 6146 x 2278 microns, Area = 14.00 sq mm



RANDY SAYS THIS CAN'T BE RIGHT (TOO BIG!)

? TRY TO LOOK AT THIS

FichtenbaumMIT

Designers:Matt Fichtenbaum
Description: A digital pulse rate monitor
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 29-Nov-79 15:05:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>FICHTENBAUMMIT.CIF;2
File creation date: 4-Dec-79 14:07:50
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

GoddeauMIT

Designers:David Goddeau, Jonathan Sieber, Chris Terman
Description: A first-in, priority-out buffer
Est.BB:3000 x 3000 microns

Space is allocated.
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
Priority time: 28-Nov-79 15:16:15
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GODDEAUMIT.CIF;2
File creation date: 4-Dec-79 0:07:02
Bounding box = 2928 x 2954 microns, Area = 8.65 sq mm

GoodrichMIT

Designers: Earl Goodrich
Description: CRT controller
Est.BB: 2000 x 1600 microns

Space is allocated.
Reserved space = 1856 x 1520 microns, Area = 2.82 sq mm
Priority time: 1-Dec-79 20:52:01
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GOODRICHMIT.CIF;2
File creation date: 4-Dec-79 12:49:03
Bounding box = 1856 x 1520 microns, Area = 2.82 sq mm

GramlichMIT

Designers: Wayne Gramlich, Carl Seaquist
Description: A writable PLA in which the programming of the AND and
OR planes is defined by contents of the static RAM cells.
Also cam program feedback loops to form finite state machines.
Est.BB: 2200 X 1700 microns.

Design is awaiting allocation.
Required space = 1524 x 1906 microns, Area = 2.90 sq mm
Priority time: 27-Nov-79 10:13:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRAMLICHMIT.CIF;2
File creation date: 29-Nov-79 19:35:37
Bounding box = 1524 x 1906 microns, Area = 2.90 sq mm

GrondalskiMIT

Designers: Robert Grondalski
Description: Writeable PLA
Est.BB: 2200 x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 28-Nov-79 7:47:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRONDALSKIMIT.CIF;2
File creation date: 4-Dec-79 13:27:20

Bounding box = 2200 x 2200 microns, Area = 4.84 sq mm

✔HamiltonMIT

Designers:Brian Hamilton
Description: Digital Alarm Clock
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 1-Dec-79 11:25:05
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>HAMILTONMIT.CIF;2
File creation date: 4-Dec-79 16:18:21
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

✔KathailMIT

Designers: Vinod Kathail, Keshav Pingali
Description: an interpreter for mapping programs onto a data flow computer
Est.BB: 2250 x 1750 microns

Design is awaiting allocation.
Required space = 1590 x 2228 microns, Area = 3.54 sq mm
Priority time: 29-Nov-79 6:01:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KATHAILMIT.CIF;3
File creation date: 4-Dec-79 15:28:28
Bounding box = 1590 x 2228 microns, Area = 3.54 sq mm

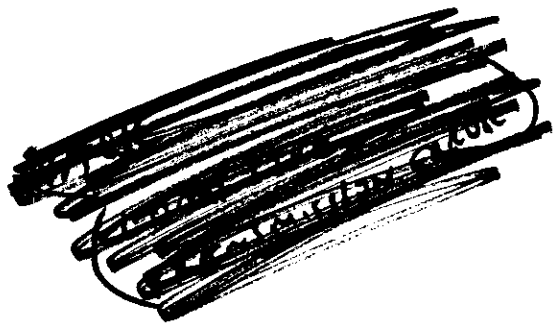
✔KhouryMIT

Designers: John Khoury
Description: Up-Down counter with programmable modulus
Est.BB: 2000 x 1725 microns

Space is allocated.
Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm
Priority time: 29-Nov-79 15:06:27
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KHOURYMIT.CIF;2
File creation date: 4-Dec-79 13:26:17
Bounding box = 2000 x 1726 microns, Area = 3.45 sq mm

✔PasemanMIT

Designers: Bill Paseman
Description: Music Synthesizer
Est.BB:4250 x 1750 microns



Space is allocated.
Reserved space = 4438 x 2944 microns, Area = 13.07 sq mm
Priority time: 30-Nov-79 13:07:25
Current submittal is not implementable.
File name: [Maxc]<MIT-VLSI>PASEMANMIT.CIF;2
File creation date: 4-Dec-79 10:17:59

✔PicardMIT

Designers: Len Picard
Description: Variable format field extractor and compactor
Est.BB: 2000 x 1750 microns

Space is allocated.
Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm
Priority time: 29-Nov-79 6:02:08
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PICARDMIT.CIF;3
File creation date: 4-Dec-79 12:50:38
Bounding box = 2000 x 1688 microns, Area = 3.38 sq mm

RivestMIT

Designers: Ron Rivest, Len Adleman, Adi Shamir
Description: Section of a Multiplier
Est.BB: 2000 x 2000

Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 29-Nov-79 6:02:47
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIVESTMIT.CIF;5
File creation date: 3-Dec-79 19:40:08
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm

M.I.T. Priorities

ONLY ONE TO QUESTION IS Chang.
IF IT LINES UP OK, DO IT.

TRY TO FIX PASEMAN.

RANDY WILL RETRANSMIT ✓ DONE O.K.

MIT

Summary of designs from MIT, updated 4-Dec-79 3:51:33

Latest scoop from REB @ 4:45

AllenMIT

Designers: Don Allen, Jerry Burchfiel
Description: Variable Length Field Decoder
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2484 x 2218 microns, Area = 5.51 sq mm
Priority time: 28-Nov-79 7:45:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>ALLENMIT.CIF;1
File creation date: 28-Nov-79 7:45:20
Bounding box = 2484 x 2218 microns, Area = 5.51 sq mm

;2

BataliMIT

Designers: John Batali
Description: Zero-Crossing Detector for Image Processing
Est.BB 2650 x 1575

Space is allocated.
Reserved space = 2626 x 1626 microns, Area = 4.27 sq mm
Priority time: 29-Nov-79 5:59:14
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BATALIMIT.CIF;2
File creation date: 29-Nov-79 5:59:14
Bounding box = 2626 x 1626 microns, Area = 4.27 sq mm

;3

BodonyMIT

Designers: Larry Bodony, Bruce Rose
Description: Logic State Analyzer
Est.BB: 4500 x 2650 microns

Space is allocated.
Reserved space = 924 x 944 microns, Area = 0.87 sq mm
Priority time: 28-Nov-79 7:45:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>BODONYMIT.CIF;1
File creation date: 28-Nov-79 7:45:43
Bounding box = 924 x 944 microns, Area = 0.87 sq mm

probable? (check recent mail)

ChangMIT

Designers: Frank Chang, Doug Williams
Description: Error-detecting block transfer oriented channel interface
Est.BB: 2500 x 5250 microns

Space is allocated.
Reserved space = 5250 x 2500 microns, Area = 13.13 sq mm
Priority time: 29-Nov-79 5:59:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHANGMIT.CIF;2
File creation date: 29-Nov-79 5:59:33
Bounding box = 5250 x 2500 microns, Area = 13.13 sq mm

;4

ChuMIT

Designers: Tam-Anh Chu, Nhi-Anh Chu, Steve McCormick
Description: Second order digital filter stage
Est.BB: 2400 x 6200 microns

Space is allocated.
Reserved space = 6146 x 2296 microns, Area = 14.11 sq mm
Priority time: 29-Nov-79 6:00:45
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>CHUMIT.CIF;2
File creation date: 29-Nov-79 6:00:45
Bounding box = 6146 x 2296 microns, Area = 14.11 sq mm

;3

FichtenbaumMIT

Designers:Matt Fichtenbaum
Description: A digital pulse rate monitor
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 29-Nov-79 15:05:20
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>FICHTENBAUMMIT.CIF;1
File creation date: 29-Nov-79 15:05:20
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

~~GandlerMIT~~

Designers: William Gandler
Description: Controller for 4 phase motor
Est.BB: 2000 x 2000 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

GoddeauMIT

Designers:David Goddeau, Jonathan Sieber, Chris Terman
Description: A first-in, priority-out buffer
Est.BB:3000 x 3000 microns

Space is allocated.
Reserved space = 2928 x 2954 microns, Area = 8.65 sq mm
Priority time: 28-Nov-79 15:16:15
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GODDEAUMIT.CIF;2
File creation date: 4-Dec-79 0:07:02
Bounding box = 2928 x 2954 microns, Area = 8.65 sq mm

GoodrichMIT

Designers: Earl Goodrich
Description: CRT controller
Est.BB: 2000 x 1600 microns

Space is allocated.
Reserved space = 1862 x 1546 microns, Area = 2.88 sq mm
Priority time: 1-Dec-79 20:52:01
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GOODRICHMIT.CIF;1
File creation date: 1-Dec-79 20:52:01
Bounding box = 1862 x 1546 microns, Area = 2.88 sq mm

GramlichMIT

Designers: Wayne Gramlich, Carl Seaquist
Description: A writable PLA in which the programming of the AND and
OR planes is defined by contents of the static RAM cells.
Also cam program feedback loops to form finite state machines.
Est.BB: 2200 X 1700 microns.

Design is awaiting allocation.
Required space = 1524 x 1906 microns, Area = 2.90 sq mm
Priority time: 27-Nov-79 10:13:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRAMLICHMIT.CIF;2
File creation date: 29-Nov-79 19:35:37
Bounding box = 1524 x 1906 microns, Area = 2.90 sq mm

GrondalskiMIT

Designers: Robert Grondalski
Description: Writeable PLA
Est.BB: 2200 x 2200 microns

Space is allocated.
Reserved space = 2200 x 2200 microns, Area = 4.84 sq mm
Priority time: 28-Nov-79 7:47:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>GRONDALSKIMIT.CIF;1
File creation date: 28-Nov-79 7:47:36
Bounding box = 2200 x 2200 microns, Area = 4.84 sq mm

HamiltonMIT

j2

Designers:Brian Hamilton
Description: Digital Alarm Clock
Est.BB: 2500 x 2500 microns

Space is allocated.
Reserved space = 2500 x 2500 microns, Area = 6.25 sq mm
Priority time: 1-Dec-79 11:25:05
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>HAMILTONMIT.CIF;1
File creation date: 1-Dec-79 11:25:05
Bounding box = 2500 x 2500 microns, Area = 6.25 sq mm

~~JangMIT~~ delete

Designers: Saquib Jang
Description: Priority storage system
Est.BB: 2500 x 1400 microns

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<MIT-VLSI>JANGMIT.CIF;1
File creation date: 28-Nov-79 7:47:59

KathailMIT

j3

Designers: Vinod Kathail, Keshav Pingali
Description: an interpreter for mapping programs onto a data flow computer
Est.BB: 2250 x 1750 microns

Space is allocated.
Reserved space = 904 x 1168 microns, Area = 1.06 sq mm
Priority time: 29-Nov-79 6:01:43
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KATHAILMIT.CIF;2
File creation date: 29-Nov-79 6:01:43
Bounding box = 904 x 1168 microns, Area = 1.06 sq mm

KhouryMIT

j2

Designers: John Khoury
Description: Up-Down counter with programmable modulus
Est.BB: 2000 x 1725 microns

Space is allocated.
Reserved space = 2000 x 1726 microns, Area = 3.45 sq mm
Priority time: 29-Nov-79 15:06:27
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>KHOURYMIT.CIF;1
File creation date: 29-Nov-79 15:06:27
Bounding box = 2000 x 1726 microns, Area = 3.45 sq mm

MayleMIT

delete

(~~probably won't make it~~)

Designers: Neil Mayle
Description: Crossbar for AI inference networks
Est.BB: 2000 x 2000 microns

Design is awaiting allocation.
Required space = 2250 x 2126 microns, Area = 4.78 sq mm
Priority time: 30-Nov-79 12:04:36
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>MAYLEMIT.CIF;2
File creation date: 3-Dec-79 10:45:41
Bounding box = 2250 x 2126 microns, Area = 4.78 sq mm

PasemanMIT ;2

Designers: Bill Paseman
Description: Music Synthesizer
Est.BB:4250 x 1750 microns

Space is allocated.
Reserved space = 4438 x 2944 microns, Area = 13.07 sq mm
Priority time: 30-Nov-79 13:07:25
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PASEMANMIT.CIF;1
File creation date: 30-Nov-79 13:07:25
Bounding box = 4438 x 2944 microns, Area = 13.07 sq mm

PicardMIT ;3

Designers: Len Picard
Description: Variable format field extractor and compactor
Est.BB: 2000 x 1750 microns

Space is allocated.
Reserved space = 2000 x 1688 microns, Area = 3.38 sq mm
Priority time: 29-Nov-79 6:02:08
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>PICARDMIT.CIF;2
File creation date: 29-Nov-79 6:02:08
Bounding box = 2000 x 1688 microns, Area = 3.38 sq mm

[redacted] delete

Designers: Andrew Ressler, Carl Hewitt, Phyliss Koton
Description: communications chip for interconnecting processors
in a multiple processor system
Est.BB: 4500 x 5200 microns

Space is allocated.
Reserved space = 5000 x 5898 microns, Area = 29.49 sq mm
Priority time: 1-Dec-79 20:52:33
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RESSLERMIT.CIF;2
File creation date: 1-Dec-79 20:52:33
Bounding box = 5000 x 5898 microns, Area = 29.49 sq mm

RiesMIT ? delete (probably want to do it)

Designers: Paul Ries
Description: Dual rail, self-timed FIFO, arbiter test circuits
Est.BB: 2000 x 2000 microns

Space is allocated.
Reserved space = 1720 x 1096 microns, Area = 1.89 sq mm
Priority time: 29-Nov-79 6:02:30
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIESMIT.CIF;2
File creation date: 29-Nov-79 6:02:30
Bounding box = 1720 x 1096 microns, Area = 1.89 sq mm

RivestMIT ;5

Designers: Ron Rivest, Len Adleman, Adi Shamir
Description: Section of a Multiplier
Est.BB: 2000 x 2000

```
Space is allocated.
Reserved space = 2250 x 2250 microns, Area = 5.06 sq mm
Priority time: 29-Nov-79  6:02:47
Current submittal is acceptable for implementation.
File name: [Maxc]<MIT-VLSI>RIVESTMIT.CIF;5
File creation date:  3-Dec-79 19:40:08
Bounding box = 2250 x 2250 microns, Area = 5.06 sq mm
----------------------------------------
```

OTHER SUMMARY

6 proj.	65.50 mm^2

(Doc chips not counted)

OTHER FINAL

Summary of designs from Other, updated 4-Dec-79 20:40:30

BoydOT

Delete

Designer: David Boyd

Design is not ready for space allocation.
No file has been submitted for implementation.

GlasserOT

Designer: Lance Glasser

Design is awaiting allocation.
Required space = 1486 x 808 microns, Area = 1.20 sq mm
Priority time: 1-Dec-79 13:31:38
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>GLASSEROT.CIF;1
File creation date: 1-Dec-79 13:31:38
Bounding box = 1486 x 808 microns, Area = 1.20 sq mm

KehlOT

Designer: Ted Kehl, Ram Rao, Ed Lazowska
Description: Address intercept logic for microcomputer
Est.BB: 1815 X 1780 microns

Design is awaiting allocation.
Required space = 1818 x 1782 microns, Area = 3.24 sq mm
Priority time: 24-Nov-79 12:28:02
Current submittal is acceptable for implementation.
File name: [maxc]<LYON>KEHLOT.CIF;1
File creation date: 24-Nov-79 12:28:02
Bounding box = 1818 x 1782 microns, Area = 3.24 sq mm

LhDoc1

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

LhDoc2

This is the left half of the document chip

Space is allocated.
Reserved space = 2918 x 4688 microns, Area = 13.68 sq mm
Priority time: 2-Dec-79 22:04:51
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>LHCHIP.CIF;1
File creation date: 2-Dec-79 22:04:51
Bounding box = 2918 x 4688 microns, Area = 13.68 sq mm

MurrayOT

Designer: John Murray

Design is awaiting allocation.
Required space = 1512 x 1642 microns, Area = 2.48 sq mm
Priority time: 3-Dec-79 11:40:27
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>MURRAYOT.CIF;1
File creation date: 3-Dec-79 11:40:27
Bounding box = 1512 x 1642 microns, Area = 2.48 sq mm

RHDoc1

This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RHCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

RHDoc2

This is the right side document chip

Space is allocated.
Reserved space = 3548 x 4424 microns, Area = 15.70 sq mm
Priority time: 2-Dec-79 22:10:48
Current submittal is acceptable for implementation.
File name: [Maxc]<M-NEWELL>RHCHIP.CIF;1
File creation date: 2-Dec-79 22:10:48
Bounding box = 3548 x 4424 microns, Area = 15.70 sq mm

RodgersOT

Designer: Mike Rodgers

Design is awaiting allocation.
Required space = 1248 x 1708 microns, Area = 2.13 sq mm
Priority time: 3-Dec-79 13:12:01
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>RODGERSOT.CIF;3
File creation date: 3-Dec-79 13:12:01
Bounding box = 1248 x 1708 microns, Area = 2.13 sq mm

Schip2

Designers: Gerry Sussman, Jack Holloway, Guy Steele, Alan Bell
Description: Lisp Microprocesser
Est.BB: 7548 X 5925 microns

ITERATE

Space is allocated.
Reserved space = 5926 x 7548 microns, Area = 44.73 sq mm
Priority time: 19-Nov-79 21:25:06
Current submittal is acceptable for implementation.
File name: [Maxc1]<ABELL>SCHIP2C.CIF;1
File creation date: 19-Nov-79 21:26:06
Bounding box = 5926 x 7548 microns, Area = 44.73 sq mm

SmithOT

Designer(s): Lee Smith, Irene Buchanan
Description: Link design
Est.BB: ~ 2000 X 1400 microns.

Delete

Design is not ready for space allocation.
No file has been submitted for implementation.

SynderOT

Designer: Larry Synder (of Yale, now at U. Wash.)
Description: A binary tree processor that computes boolean functions, with inputs at the leaves and at the root.
Est.BB: 3420 x 3470 microns

Design is awaiting allocation.
Required space = 3418 x 3430 microns, Area = 11.72 sq mm
Priority time: 27-Nov-79 18:49:56

```
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>SNYDEROT.CIF;1
File creation date:  3-Dec-79 11:23:20
Bounding box = 3418 x 3430 microns, Area = 11.72 sq mm
----------------------------------------
```

Memo from: LYNN CONWAY

U of R Summary

5 proj.	30.34 mm^2

XEROX

UofR FINAL

Summary of designs from UofR, updated 4-Dec-79 23:13:17

✔ KedemUR

Designers(s): Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Est.BB: ~ 2000 x 2000 microns.

Design is awaiting allocation.
Required space = 2698 x 2786 microns, Area = 7.52 sq mm
Priority time: 4-Dec-79 20:06:31
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>KEDEMUR.CIF;1
File creation date: 4-Dec-79 20:06:31
Bounding box = 2698 x 2786 microns, Area = 7.52 sq mm

✔ LyonsUR

Implementer: Bob Lyons
Description: Programmable Frequency Generator
Est.BB: 3000 microns x 3000 microns

Design is awaiting allocation.
Required space = 2748 x 2276 microns, Area = 6.25 sq mm
Priority time: 4-Dec-79 20:04:24
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>LYONSUR.CIF;2
File creation date: 4-Dec-79 20:04:24
Bounding box = 2748 x 2276 microns, Area = 6.25 sq mm

✔ SohmUR

Designers: Larry Sohm, Pat Chan, Bill Notowitz
Description: Digital Phase lock loop
Est.BB: 1500 x 3000 microns.

Design is awaiting allocation.
Required space = 3610 x 2634 microns, Area = 9.51 sq mm
Priority time: 4-Dec-79 19:06:24
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>SOHMUR.CIF;2
File creation date: 4-Dec-79 19:06:24
Bounding box = 3610 x 2634 microns, Area = 9.51 sq mm

✔ TiloveUR

Designer(s): Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Est. BB: ~ 1400 X 2000 microns.

Design is awaiting allocation.
Required space = 1934 x 1326 microns, Area = 2.56 sq mm
Priority time: 4-Dec-79 18:39:39
Current submittal is acceptable for implementation.
File name: [Maxc]<LYON>TILOVEUR.CIF;1
File creation date: 4-Dec-79 18:39:39
Bounding box = 1934 x 1326 microns, Area = 2.56 sq mm

✔ WatanabeUR

Designer: Yuki Watanabe
Description: Sorter slice
Est.BB: 2300 x 2600 micron

Design is awaiting allocation.
Required space = 2008 x 2240 microns, Area = 4.50 sq mm
Priority time: 4-Dec-79 19:09:22
Current submittal is acceptable for implementation.
File name: [Maxc]<UOFR-VLSI>WATANABEUR.CIF;2
File creation date: 4-Dec-79 19:09:22
Bounding box = 2008 x 2240 microns, Area = 4.50 sq mm

UofR

Summary of designs from UofR, updated 4-Dec-79 3:51:33

ErmerUR

Implementer: Rick Ermer and Tuan Nguyen
Description: Speedometer/Odometer
Est.BB: 2000 microns x 3750 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

KahrsUR

Designer: Mark Kahrs
Description: 13 bit DAC
Est.BB: 2500 x 1500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

KedemUR

Designers(s): Gershon Kedem and Michel Denber
Description: Infinite precision multiplier
Est.BB: ~ 2000 x 2000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

LylesUR

Implementer: Brian Lyles
Description: Interpolative A/D
Est.BB: 2000 microns x 1250 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

LyonsUR

Implementer: Bob Lyons
Description: Programmable Frequency Generator
Est.BB: 3000 microns x 3000 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

RajUR

Implementer: Raj
Description: CAM
Est.BB: 2000 microns x 500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

SabbahUR

Designer: Danny Sabbah
Description: Programmable SLA
Est.BB: ~ 4600 x 5500 microns

Design is not ready for space allocation.
No file has been submitted for implementation.

SohmUR

Designers: Larry Sohm, Pat Chan, Bill Notowitz

Description: Digital Phase lock loop
Est.BB: 1500 x 3000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

TiloveUR

Designer(s): Bob Tilove, Jarek Rossignac
Description: This is a bit slice coordinate transformer
Est. BB: ~ 1400 X 2000 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

UofR Priority:

- Watanabe
- Kelley — on [Marc] <Lyon>
- Lyons
- Sohns

- TiloverUR.CIF — on [Marc] <Lyon>

Sabbah — Some calculations. Figuratively wasteful of space

Kahrs	N.G.
Lyles	N.G.
Raj	N.G.

Memo from: LYNN CONWAY

SU SUMMARY:

19 proj.	79.16 mm²

+ HIT LIST:

5 proj. 28.66 mm²

3

XEROX

SU FINAL

Summary of designs from SU, updated 4-Dec-79 20:40:30

✓ AtlasSU

Designer(s): Les Atlas, Doug Galbraith
Description: This project is an neural-stim. interval timer
Est.BB: ~ 2500 x 2000 microns. *

Space is allocated.
Reserved space = 2478 x 1378 microns, Area = 3.41 sq mm
Priority time: 30-Nov-79 23:42:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ATLASSU.CIF;4
File creation date: 4-Dec-79 16:28:09
Bounding box = 2478 x 1378 microns, Area = 3.41 sq mm

✓ BasкettSU

Designer(s): Forest Baskett
Description: This project is an Ethernet synchronizer
Est.BB: ~ 2250 X 2500 microns.

Space is allocated.
Reserved space = 2240 x 2720 microns, Area = 6.09 sq mm
Priority time: 26-Nov-79 8:52:03
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BASKETTSU.CIF;1
File creation date: 26-Nov-79 8:52:03
Bounding box = 2240 x 2720 microns, Area = 6.09 sq mm

✓ BectolsheimSU

Designer(s): Andy Bechtolsheim, Thomas Gross
Description: This project is a parallel search table for log arithmetic
Est.BB: ~ 3500 X 1800 microns.

Space is allocated.
Reserved space = 1514 x 3180 microns, Area = 4.81 sq mm
Priority time: 23-Nov-79 15:41:04
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BECTOLSHEIMSU.CIF;3
File creation date: 3-Dec-79 22:52:06
Bounding box = 1514 x 3180 microns, Area = 4.81 sq mm

✓ Clark2SU

Designer(s): Jim Clark
Description: This project is a self-timed clock element
Est BB: ~ 1200 x 1200 microns.

Design is awaiting allocation.
Required space = 1606 x 1688 microns, Area = 2.71 sq mm
Priority time: 1-Dec-79 19:02:59
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARK2SU.CIF;3
File creation date: 4-Dec-79 13:21:54
Bounding box = 1606 x 1688 microns, Area = 2.71 sq mm

✓ ClarkSU

Designer(s): Jim Clark
Description: This project is a simple graphics ALU
Est.BB: ~ 3000 x 3000 microns

Space is allocated.
Reserved space = 2976 x 2764 microns, Area = 8.23 sq mm
Priority time: 28-Nov-79 14:57:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARKSU.CIF;3
File creation date: 4-Dec-79 16:18:37
Bounding box = 2976 x 2764 microns, Area = 8.23 sq mm

ElahianSU

Designer(s): Kamran Elahian, Fred Basham
Description: This project is a UART line speed determiner
Est.BB: ~ 1950 X 1900 microns.

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 1-Dec-79 16:11:10
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ELAHIANSU.CIF;3
File creation date: 4-Dec-79 15:34:00
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

FrolikSU

Designer(s): Bill Frolik, Roderick Young
Description: This project is a digital timer
Est.BB: ~ 2750 x 2125 microns. *

Design is awaiting allocation.
Required space = 2120 x 2684 microns, Area = 5.69 sq mm
Priority time: 4-Dec-79 12:08:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>FROLIKSU.CIF;5
File creation date: 4-Dec-79 12:08:07
Bounding box = 2120 x 2684 microns, Area = 5.69 sq mm

GehlbachSU

Designer(s): Steve Gehlbach, Joe Sharp, Bill Jansen
Description: This project is a fast 16-input adder
Est.BB: ~ 1250 X 3250 microns. *

Space is allocated.
Reserved space = 3180 x 1856 microns, Area = 5.90 sq mm
Priority time: 30-Nov-79 8:36:06
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GEHLBACHSU.CIF;6
File creation date: 4-Dec-79 11:49:07
Bounding box = 3180 x 1856 microns, Area = 5.90 sq mm

HannahSU

Designer(s): Peter Eichenberger, Marc Hannah
Description: This project is a rectangle generator
Est.BB: ~ 2000 X 2500 microns.

Space is allocated.
Reserved space = 2386 x 2140 microns, Area = 5.11 sq mm
Priority time: 30-Nov-79 21:33:31
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HANNAHSU.CIF;6
File creation date: 4-Dec-79 12:09:11
Bounding box = 2386 x 2140 microns, Area = 5.11 sq mm

HerndonSU

Designer(s): Matt Herndon, Jeff Thorson
Description: This project is a typesetting machine
Est.BB: ~ 2500 X 2250 microns.

Space is allocated.
Reserved space = 3170 x 2000 microns, Area = 6.34 sq mm
Priority time: 30-Nov-79 23:45:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HERNDONSU.CIF;2
File creation date: 3-Dec-79 22:42:50
Bounding box = 3170 x 2000 microns, Area = 6.34 sq mm

✔ MacomberSU

Designer(s): Scott Macomber, Bob Clark
Description: This project is a parallel/serial multiplier
Est.BB: ~ 1900 X 1900 microns.

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 2-Dec-79 22:18:27
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MACOMBERSU.CIF;4
File creation date: 4-Dec-79 11:50:29
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

✔ MarkeeSU

Designer(s): Pat Markee, Irene Watson
Description: This project is a digital clock
Est.BB: ~ 2000 X 3000 microns.

Space is allocated.
Reserved space = 2120 x 1424 microns, Area = 3.02 sq mm
Priority time: 30-Nov-79 21:52:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MARKEESU.CIF;2
File creation date: 4-Dec-79 15:38:53
Bounding box = 2120 x 1424 microns, Area = 3.02 sq mm

✔ MathewsSU

Designer(s): Rob Mathews, John Newkirk
Desciption: This project is the infamous Buffalo chip
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm
Priority time: 23-Nov-79 15:33:45
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MATHEWSSU.CIF;1
File creation date: 23-Nov-79 15:33:45
Bounding box = 5180 x 1134 microns, Area = 5.87 sq mm

✔ NoiceSU

Designer(s): David Noice, Neil Midkiff
Description: This project is a multiplier/divider
Est.BB: ~ 2750 X 1500 microns.

Space is allocated.
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm
Priority time: 1-Dec-79 16:14:51
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>NOICESU.CIF;2
File creation date: 4-Dec-79 15:20:56
Bounding box = 2888 x 1576 microns, Area = 4.55 sq mm

✔ OhChinSU

Designer(s): Soo-Young Oh, Dae-Je Chin
Description: This project is a automatic thermostat time controler
Est.BB: ~ 2150 X 1600 microns.

Space is allocated.
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm
Priority time: 30-Nov-79 8:33:40
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OHCHINSU.CIF;3
File creation date: 4-Dec-79 9:02:42
Bounding box = 2120 x 1700 microns, Area = 3.60 sq mm

OyeSU HIT

Designer(s): Kevin Oye, Alan Siegel
Description: This project is a error-correcting parallel/serial interface
Est.BB: ~ 3000 X 2500 microns.

Design is awaiting allocation.
Required space = 1882 x 1486 microns, Area = 2.80 sq mm
Priority time: 4-Dec-79 17:00:38
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OYESU.CIF;2
File creation date: 4-Dec-79 17:00:38
Bounding box = 1882 x 1486 microns, Area = 2.80 sq mm

StrongSU HIT

Designer(s): Alex Strong, Danny Sleator
Description: This project is a guitar chip
Est.BB: ~ 3000 X 1875 microns.

Design is awaiting allocation.
Required space = 1856 x 2120 microns, Area = 3.93 sq mm
Priority time: 4-Dec-79 17:03:35
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>STRONGSU.CIF;4
File creation date: 4-Dec-79 17:03:35
Bounding box = 1856 x 2120 microns, Area = 3.93 sq mm

SytwuSU HIT

Designer(s): J. Sytwu, Hamid Najafi
Description: This project is a quad PCM bus interface
Est.BB: ~ 3000 X 3000 microns.

Space is allocated.
Reserved space = 4150 x 3146 microns, Area = 13.06 sq mm
Priority time: 1-Dec-79 12:36:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>SYTWUSU.CIF;2
File creation date: 4-Dec-79 16:55:21
Bounding box = 4150 x 3146 microns, Area = 13.06 sq mm

✓ TarsiSU HIT

Designer(s): Mike Tarsi, Nagatsugu Yamanouchi
Description: This project is a multifunction digital clock
Est.BB: ~ 1920 X 1920 microns.

Design is awaiting allocation.
Required space = 2140 x 2276 microns, Area = 4.87 sq mm
Priority time: 1-Dec-79 12:56:09
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>TARSISU.CIF;3
File creation date: 4-Dec-79 12:10:50
Bounding box = 2140 x 2276 microns, Area = 4.87 sq mm

✓ UttSU HIT

Designer(s): Steve Utt, Shalom Ackelsberg
Description: This project is part of a pancreas prosthesis
Est B.B.: 2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 1-Dec-79 12:56:46
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>UTTSU.CIF;3
File creation date: 4-Dec-79 11:55:45
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

✓ WulffSU

Designer(s): Bob Wulff, Tom Bennett
Description: This project is a bit slice of a multiplier
Est.BB: ~ 2375 X 2125 microns.

Design is awaiting allocation.
Required space = 2120 x 1856 microns, Area = 3.93 sq mm
Priority time: 3-Dec-79 20:31:30
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>WULFFSU.CIF;3
File creation date: 4-Dec-79 12:12:38
Bounding box = 2120 x 1856 microns, Area = 3.93 sq mm

✓ ZarghanSU

Designer(s): Bahman Zargham, Jerry Huck
Description: This project is a multiplexed communications link
Est.BB: ~ 2250 X 1900 microns.

Space is allocated.
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm
Priority time: 30-Nov-79 21:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ZARGHANSU.CIF;4
File creation date: 3-Dec-79 23:03:11
Bounding box = 1590 x 1550 microns, Area = 2.46 sq mm

SU

Summary of designs from SU, updated 4-Dec-79 3:51:33

AhmedSU

Designer(s): Hassan Ahmed, Rich Baker
Description: This project is a forward error-correction codec
Est.BB: ~ 1250 X 2250 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

AtlasSU

Designer(s): Les Atlas, Doug Galbraith
Description: This project is an neural-stim. interval timer
Est.BB: ~ 2500 x 2000 microns. *

Space is allocated.
Reserved space = 2478 x 1378 microns, Area = 3.41 sq mm
Priority time: 30-Nov-79 23:42:48
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ATLASSU.CIF;3
File creation date: 3-Dec-79 22:37:44
Bounding box = 2478 x 1378 microns, Area = 3.41 sq mm

BaskettSU

Designer(s): Forest Baskett
Description: This project is an Ethernet synchronizer
Est.BB: ~ 2250 X 2500 microns.

Space is allocated.
Reserved space = 2240 x 2720 microns, Area = 6.09 sq mm
Priority time: 26-Nov-79 8:52:03
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BASKETTSU.CIF;1
File creation date: 26-Nov-79 8:52:03
Bounding box = 2240 x 2720 microns, Area = 6.09 sq mm

BectolsheimSU

Designer(s): Andy Bechtolsheim, Thomas Gross
Description: This project is a parallel search table for log arithmetic
Est.BB: ~ 3500 X 1800 microns.

Space is allocated.
Reserved space = 1514 x 3180 microns, Area = 4.81 sq mm
Priority time: 23-Nov-79 15:41:04
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>BECTOLSHEIMSU.CIF;3
File creation date: 3-Dec-79 22:52:06
Bounding box = 1514 x 3180 microns, Area = 4.81 sq mm

Clark2SU

Designer(s): Jim Clark
Description: This project is a self-timed clock element
Est BB: ~ 1200 x 1200 microns.

Space is allocated.
Reserved space = 1630 x 1642 microns, Area = 2.68 sq mm
Priority time: 1-Dec-79 19:02:59
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARK2SU.CIF;2
File creation date: 3-Dec-79 0:09:46
Bounding box = 1630 x 1642 microns, Area = 2.68 sq mm

ClarkSU

Designer(s): Jim Clark

Description: This project is a simple graphics ALU
Est.BB: ~ 3000 x 3000 microns

Space is allocated.
Reserved space = 2764 x 2976 microns, Area = 8.23 sq mm
Priority time: 28-Nov-79 14:57:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>CLARKSU.CIF;1
File creation date: 28-Nov-79 14:57:42
Bounding box = 2764 x 2976 microns, Area = 8.23 sq mm

ElahianSU

Designer(s): Kamran Elahian, Fred Basham
Description: This project is a UART line speed determiner
Est.BB: ~ 1950 X 1900 microns.

Space is allocated.
Reserved space = 1856 x 1856 microns, Area = 3.44 sq mm
Priority time: 1-Dec-79 16:11:10
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ELAHIANSU.CIF;2
File creation date: 3-Dec-79 22:59:42
Bounding box = 1856 x 1856 microns, Area = 3.44 sq mm

ErbilSU

Designer(s): Oktay Erbil, Peter Fu
Description: This project is a consistency unit for a fault-tolerant system
Est.BB: ~ 2250 X 1950 microns.

Space is allocated.
Reserved space = 2250 x 2500 microns, Area = 5.63 sq mm
Priority time: 2-Dec-79 22:17:37
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ERBILSU.CIF;2
File creation date: 2-Dec-79 22:17:37
Bounding box = 2250 x 2500 microns, Area = 5.63 sq mm

FrolikSU

Designer(s): Bill Frolik, Roderick Young
Description: This project is a digital timer
Est.BB: ~ 2750 x 2125 microns. *

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<SU-VLSI>FROLIKSU.CIF;4
File creation date: 1-Dec-79 15:49:41

GehlbachSU

Designer(s): Steve Gehlbach, Joe Sharp, Bill Jansen
Description: This project is a fast 16-input adder
Est.BB: ~ 1250 X 3250 microns. *

Space is allocated.
Reserved space = 3180 x 1856 microns, Area = 5.90 sq mm
Priority time: 30-Nov-79 8:36:06
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GEHLBACHSU.CIF;5
File creation date: 3-Dec-79 9:30:45
Bounding box = 3180 x 1856 microns, Area = 5.90 sq mm

GlussSU

Designer(s): Dave Gluss, Bill Nowicki
Description: This project is a Ethernet deserializing buffer
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.

Reserved space = 3180 x 1644 microns, Area = 5.23 sq mm
Priority time: 1-Dec-79 12:31:33
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>GLUSSSU.CIF;1
File creation date: 1-Dec-79 12:31:33
Bounding box = 3180 x 1644 microns, Area = 5.23 sq mm

HannahSU

Designer(s): Peter Eichenberger, Marc Hannah
Description: This project is a rectangle generator
Est.BB: ~ 2000 X 2500 microns.

Space is allocated.
Reserved space = 2386 x 2140 microns, Area = 5.11 sq mm
Priority time: 30-Nov-79 21:33:31
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HANNAHSU.CIF;6
File creation date: 3-Dec-79 16:43:58
Bounding box = 2386 x 2140 microns, Area = 5.11 sq mm

HerndonSU

Designer(s): Matt Herndon, Jeff Thorson
Description: This project is a typesetting machine
Est.BB: ~ 2500 X 2250 microns.

Space is allocated.
Reserved space = 3170 x 2000 microns, Area = 6.34 sq mm
Priority time: 30-Nov-79 23:45:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HERNDONSU.CIF;2
File creation date: 3-Dec-79 22:42:50
Bounding box = 3170 x 2000 microns, Area = 6.34 sq mm

HorowitzSU

Designer(s): Mark Horowitz, Wayne Wolf
Description: This project is a model train speed controller
Est.BB: ~ 2000 X 2125 microns.

Design is awaiting allocation.
Required space = 2430 x 2160 microns, Area = 5.25 sq mm
Priority time: 3-Dec-79 20:29:55
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HOROWITZSU.CIF;2
File creation date: 3-Dec-79 20:29:55
Bounding box = 2430 x 2160 microns, Area = 5.25 sq mm

HuangSU

Designer(s): Wen-her Huang
Description: This project is a CAM
Est.BB: ~ 2000 X 2000 microns.

Design is awaiting allocation.
Required space = 2100 x 2000 microns, Area = 4.20 sq mm
Priority time: 3-Dec-79 16:45:54
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>HUANGSU.CIF;1
File creation date: 3-Dec-79 16:45:54
Bounding box = 2100 x 2000 microns, Area = 4.20 sq mm

KarmarkarSU

Designer(s): Narendra Karmarkar, Timothy Gonsalves
Description: This project is a bit-slice residue autocorrelator
Est.BB: ~ 2000 X 2125 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

MacomberSU

Designer(s): Scott Macomber, Bob Clark
Description: This project is a parallel/serial multiplier
Est.BB: ~ 1900 X 1900 microns.

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm
Priority time: 2-Dec-79 22:18:27
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MACOMBERSU.CIF;3
File creation date: 2-Dec-79 22:18:27
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

MarkeeSU

Designer(s): Pat Markee, Irene Watson
Description: This project is a digital clock
Est.BB: ~ 2000 X 3000 microns.

Space is allocated.
Reserved space = 2120 x 1424 microns, Area = 3.02 sq mm
Priority time: 30-Nov-79 21:52:42
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MARKEESU.CIF;1
File creation date: 30-Nov-79 21:52:42
Bounding box = 2120 x 1424 microns, Area = 3.02 sq mm

MathewsSU

Designer(s): Rob Mathews, John Newkirk
Desciption: This project is the infamous Buffalo chip
Est.BB: ~ 5000 X 1250 microns.

Space is allocated.
Reserved space = 5180 x 1134 microns, Area = 5.87 sq mm
Priority time: 23-Nov-79 15:33:45
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>MATHEWSSU.CIF;1
File creation date: 23-Nov-79 15:33:45
Bounding box = 5180 x 1134 microns, Area = 5.87 sq mm

NoiceSU

Designer(s): David Noice, Neil Midkiff
Description: This project is a multiplier/divider
Est.BB: ~ 2750 X 1500 microns.

Space is allocated.
Reserved space = 2888 x 1576 microns, Area = 4.55 sq mm
Priority time: 1-Dec-79 16:14:51
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>NOICESU.CIF;1
File creation date: 1-Dec-79 16:14:51
Bounding box = 2888 x 1576 microns, Area = 4.55 sq mm

OhChinSU

Designer(s): Soo-Young Oh, Dae-Je Chin
Description: This project is a automatic thermostat time controler
Est.BB: ~ 2150 X 1600 microns.

Space is allocated.
Reserved space = 2120 x 1700 microns, Area = 3.60 sq mm
Priority time: 30-Nov-79 8:33:40
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>OHCHINSU.CIF;2
File creation date: 30-Nov-79 8:33:40
Bounding box = 2120 x 1700 microns, Area = 3.60 sq mm

OyeSU

Designer(s): Kevin Oye, Alan Siegel
Description: This project is a error-correcting parallel/serial interface
Est.BB: ~ 3000 X 2500 microns.

Design is not ready for space allocation.
No file has been submitted for implementation.

RedfordSU

Designer(s): John Redford, Lyle Smith
Description: This project is a self test memory
Est.BB: ~ 3125 x 2875 microns

Space is allocated.
Reserved space = 2126 x 2776 microns, Area = 5.90 sq mm
Priority time: 1-Dec-79 12:33:37
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>REDFORDSU.CIF;1
File creation date: 1-Dec-79 12:33:37
Bounding box = 2126 x 2776 microns, Area = 5.90 sq mm

StrongSU

Designer(s): Alex Strong, Danny Sleator
Description: This project is a guitar chip
Est.BB: ~ 3000 X 1875 microns.

Design is not ready for space allocation.
Current submittal is not implementable.
File name: [Maxc]<SU-VLSI>STRONGSU.CIF;2
File creation date: 1-Dec-79 15:45:03

SytwuSU

Designer(s): J. Sytwu, Hamid Najafi
Description: This project is a quad PCM bus interface
Est.BB: ~ 3000 X 3000 microns.

Space is allocated.
Reserved space = 3000 x 2546 microns, Area = 7.64 sq mm
Priority time: 1-Dec-79 12:36:07
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>SYTWUSU.CIF;1
File creation date: 1-Dec-79 12:36:07
Bounding box = 3000 x 2546 microns, Area = 7.64 sq mm

TarsiSU

Designer(s): Mike Tarsi, Nagatsugu Yamanouchi
Description: This project is a multifunction digital clock
Est.BB: ~ 1920 X 1920 microns.

Design is awaiting allocation.
Required space = 2140 x 2276 microns, Area = 4.87 sq mm
Priority time: 1-Dec-79 12:56:09
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>TARSISU.CIF;2
File creation date: 3-Dec-79 16:46:34
Bounding box = 2140 x 2276 microns, Area = 4.87 sq mm

UttSU

Designer(s): Steve Utt, Shalom Ackelsberg
Description: This project is part of a pancreas prosthesis
Est B.B.: 2000 X 2000 microns

Space is allocated.
Reserved space = 2000 x 2000 microns, Area = 4.00 sq mm

Priority time: 1-Dec-79 12:56:46
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>UTTSU.CIF;2
File creation date: 1-Dec-79 12:56:46
Bounding box = 2000 x 2000 microns, Area = 4.00 sq mm

WulffSU

Designer(s): Bob Wulff, Tom Bennett
Description: This project is a bit slice of a multiplier
Est.BB: ~ 2375 X 2125 microns.

Design is awaiting allocation.
Required space = 2120 x 1856 microns, Area = 3.93 sq mm
Priority time: 3-Dec-79 20:31:30
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>WULFFSU.CIF;2
File creation date: 3-Dec-79 20:31:30
Bounding box = 2120 x 1856 microns, Area = 3.93 sq mm

ZarghanSU

Designer(s): Bahman Zargham, Jerry Huck
Description: This project is a multiplexed communications link
Est.BB: ~ 2250 X 1900 microns.

Space is allocated.
Reserved space = 1590 x 1550 microns, Area = 2.46 sq mm
Priority time: 30-Nov-79 21:36:20
Current submittal is acceptable for implementation.
File name: [Maxc]<SU-VLSI>ZARGHANSU.CIF;4
File creation date: 3-Dec-79 23:03:11
Bounding box = 1590 x 1550 microns, Area = 2.46 sq mm

SU Priorities

(1) M. Trews, Baskett, Bechtolsheim, Clark

(2) Atlas, Herndon, Noire, OhChin, Frolik, Hannah, Gehlbach, Macomber, Elahian, Wulff, Zarghan

(3) Markee, Utt, Tarpi

(4) Sytwu

(5) Oye, Strong

(494-2959)

HIT